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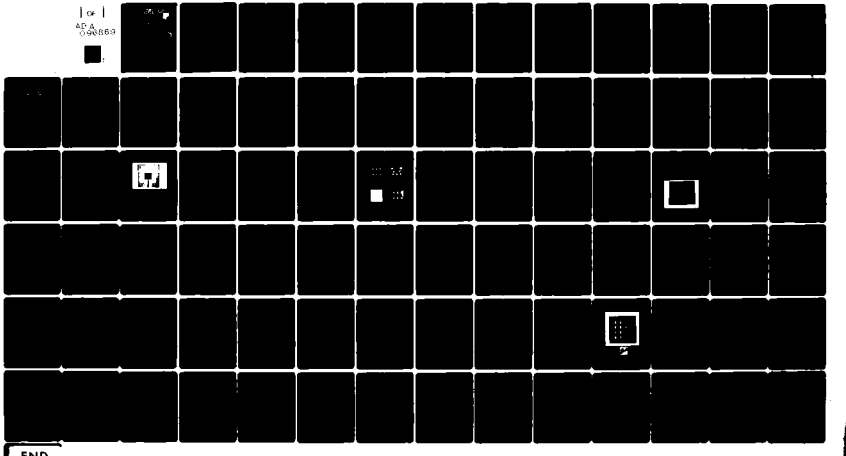

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Final Technical Report
February 1981

15 GHz MICROSTRIP ARRAY DEVELOPMENT

Ball Aerospace Systems Division

Ron Stockton
Marguerite M. Balint

ROME AIR DEVELOPMENT CENTER
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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

An investigation of the feasibility of electronically scannable microstrip phased array antennas operating in the 15 GHz region was accomplished. Monolithic, multi-layer and modular approaches were analyzed and their expected performance capabilities, cost, weight, and other factors were compared. In addition, a prototype model of a preferred array design was fabricated and tested.

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EVALUATION

This final report contains information comparing the performance, cost and weight of several techniques that can be used to fabricate microstrip antenna phased arrays at 15 GHz. A great deal of background information on the various techniques is included to supplement the tabulated data. The problems inherent in fabricating 15 GHz arrays on a high dielectric sapphire substrate are outlined and modifications to standard construction techniques that alleviate these are proposed and experimentally verified.

JOHN McILVENNA
Project Engineer

SUMMARY

One way to improve jamming and intercept immunity of communication links without penalizing channel capacity, is to use frequencies in the 15 GHz band in conjunction with phased array antennas for greater directional agility. In view of the successful development of microstrip phased arrays at X-band, there is a strong interest in extending the operating frequency of these conformal, low profile antennas.

The objective of this program was to investigate and compare a variety of construction techniques with respect to performance, cost, weight and ease of fabrication. The most suitable approach was chosen for fabrication and test as a breadboard model.

During the analysis phase, monolithic, monolithic/hybrid, multi-layer and modular design concepts on both high and low dielectric constant materials were evaluated for implementation. Although the materials and fabrication techniques differ substantially, we were surprised to find that the overall efficiency of the baseline 8x8 arrays differed by less than 12 percent while the projected costs varied by more than an order of magnitude. In addition, microstrip radiators were designed and tested on teflon-fiberglass, quartz, and sapphire dielectric materials with efficiencies of 95 percent. Although the all monolithic array concept offered significant repeatability, reliability and cost advantages and a potential for comparable performance with respect to the other candidate designs, this approach could not be implemented on this program in view of the extensive process development effort required. Therefore, the monolithic/hybrid approach on sapphire was selected for breadboard fabrication.

Regrettably, our attempts to implement a 4x4 element breadboard phased array were unsuccessful. Due to the high dielectric constant of sapphire

(9.39) and the 15 GHz operating frequency, it was necessary to employ precision masks and photoetch procedures to create and reproduce geometries with dimensions between .001 and 0.01 inch. Because of the long fabrication times associated with this precision requirement, the complete development of a 15 GHz 3-bit phase shifter was not accomplished. However, a series of experiments that resulted in acceptable element, array, power divider and 3-dB branch-line coupler were conducted and lend insight into the fabrication of 15 GHz microstrip arrays on high dielectric constant materials.

PREFACE

This final report, prepared by Ball Aerospace Systems Division (BASD), Boulder, Colorado, contains the results of a developmental study conducted at BASD between March 1, 1979 and May 31, 1980, under Air Force Contract No. F30602-79-C-0114.

The purpose of this study was to investigate design concepts and fabrication techniques for microstrip phased arrays at 15 GHz. This work was a continuation of a previous AFSC Contract entitled "Microstrip Phased Array Antennas," Contract No. F30602-75-C-0137.

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1.0 ARRAY INVESTIGATION

Fabrication techniques for microstrip phased arrays at 15 GHz were investigated in detail. Initially, a qualitative assessment of each approach was conducted to determine the inherent advantages and disadvantages of the concept. This preliminary survey was followed by a rigorous quantitative analysis to determine performance estimates and size, weight and cost tradeoffs. The results of the array investigation are presented in the following section.

1.1 Description of Fabrication Techniques

1.1.1 Monolithic/Hybrid Approach

The monolithic/hybrid approach is a standard construction method for microstrip phased arrays. The term monolithic refers to the thin conformal conductor layer supported by a dielectic material. This layer contains the radiating elements, feed network, phase shifter circuitry, DC bias chokes, and DC bias lines. These transmission line components are fabricated simultaneously using a single photolithographic process.

The array is completed by installing the semiconductor phase shifter control elements (typically PIN diode chips) on the photoetched conductors. The addition of the discrete components on the monolithic radiating aperture essentially creates a large hybrid circuit; hence, the term monolithic/hybrid was adopted to describe this approach. An example of a monolithic/hybrid phased array is shown in Figure 1.

1.1.2 Monolithic Approach

A viable alternative to the monolithic/hybrid approach is a true monolithic structure in which the semiconductor components are

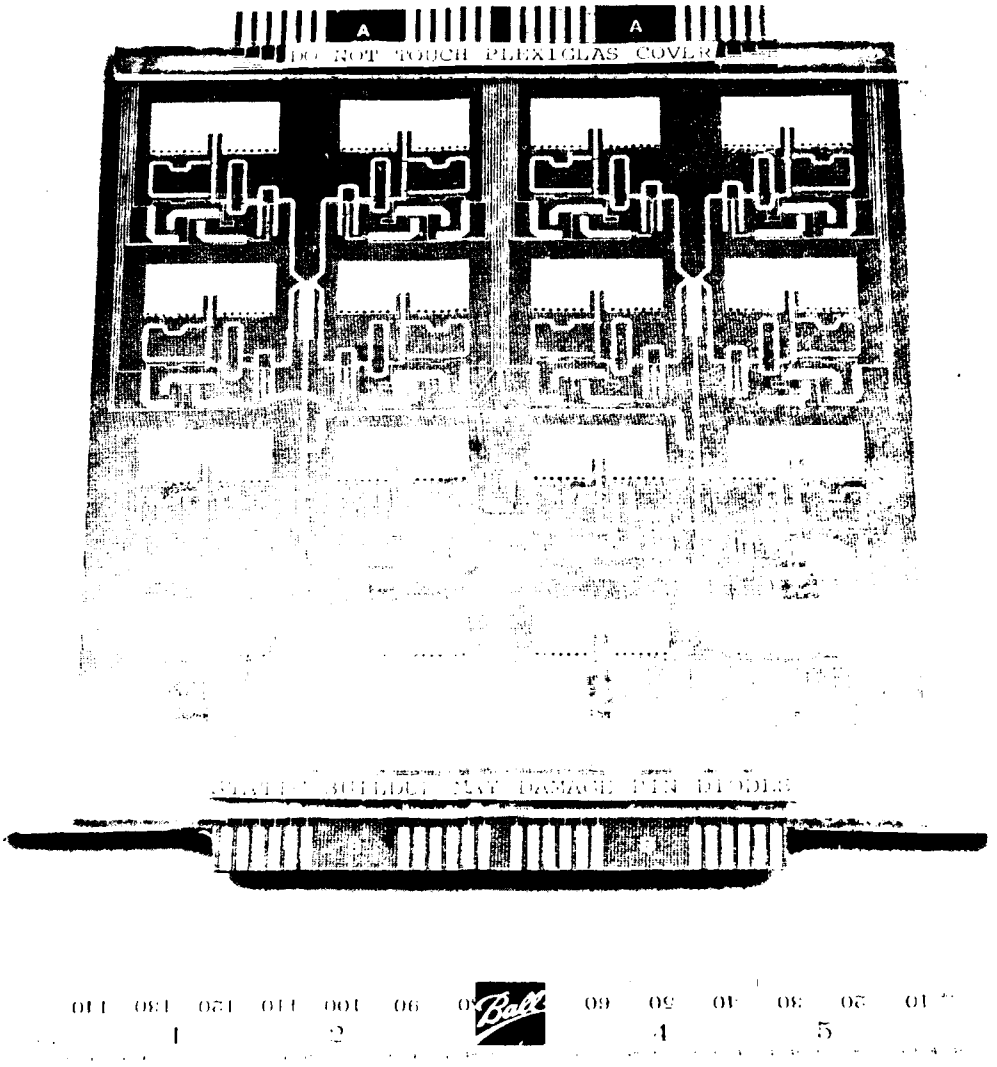


Figure 1. Typical Monolithic/Hybrid Construction

fabricated in-situ on the aperture substrate. Although this concept of a Monolithic Microwave Integrated Antenna (MMIA) has not yet been reduced to practice, the technique is included in view of its potential benefits and probable near-term implementation.

1.1.3 Multi-Layer Approach

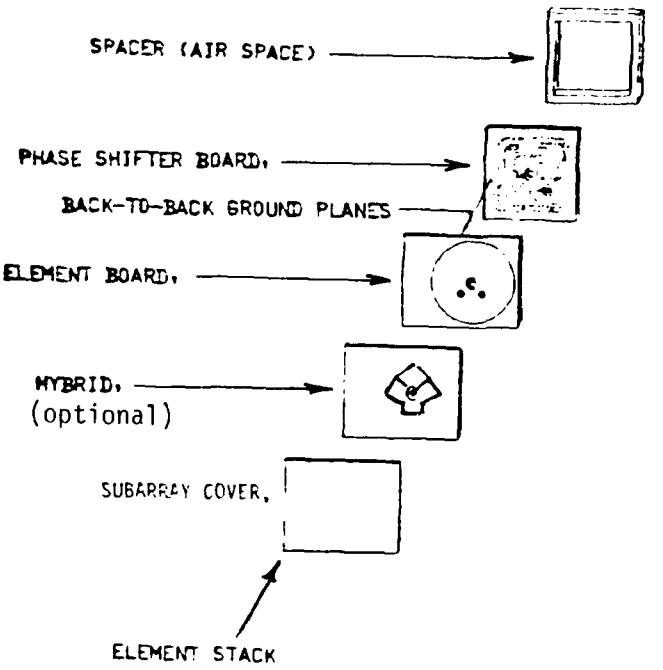
A multi-layer approach is another standard construction technique for microstrip phased arrays. In general, the radiating elements are fabricated on the top layer while a second, lower layer contains the feed network and phase shifters. Since both layers typically use microstrip construction, the two RF boards are mounted back to back (ground plane to ground plane) and interconnected with feed-through pins. An additional layer may be included to support the attendant digital control electronics and DC power distribution adjacent to the antenna array. An example of this construction technique is illustrated in Figure 2.

1.1.4 Modular Approach

The modular approach implies that a multiplicity of phase shifters are fabricated on a high dielectric substrate using hybrid circuit technology. This substrate can either be integrated into the aperture as an insert or as separate layer in a multilayer structure.

1.2 Qualitative Assessment of Candidate Designs

The objective of the analysis phase was to compare the various design concepts with respect to performance, cost, weight, and ease of fabrication. Our approach to this task included an initial qualitative assessment in which the inherent advantages and disadvantages of each design were summarized, followed by a com-



Each layer contains 64 of the devices indicated for a complete 8x8 array.

Figure 2. Typical Multi Layer Construction

prehensive quantitative analysis to determine the magnitude, hence the significance of the strong and weak points. Each candidate design concept is evaluated in terms of its advantages and disadvantages.

1.2.1 Monolithic/Hybrid on Low K Material

The monolithic/hybrid approach on low dielectric constant materials ($\varepsilon < 3$) such as teflon-fiberglass laminates has been a standard construction technique for microstrip phased arrays for many years. The principal benefits of this design are its moderate simplicity, lightweight, and ability to conform to a curved surface. All of these desirable characteristics are directly related to the one layer, single photoetch process fabrication procedure.

The design, however, is not without drawbacks on low dielectric constant materials. For functional implementation the phase shifters, corporate feed and DC control lines are interspersed between the radiating elements. In an array lattice with 0.5 λo element spacing as shown in Figure 3, the available inter-element surface area is given by equation (1):

$$A = (0.5\lambda o)^2 - (0.5\lambda d)^2 \text{ where } \lambda o = \sqrt{\varepsilon_r}\lambda d. \qquad (1)$$

For a typical teflon-fiberglass plastic laminate, $\varepsilon_r = 2.4$, the above expression reduces to

$$A = 0.146\ \lambda o^2 \quad \text{or} \quad 0.35\ \lambda d^2 \qquad (2)$$

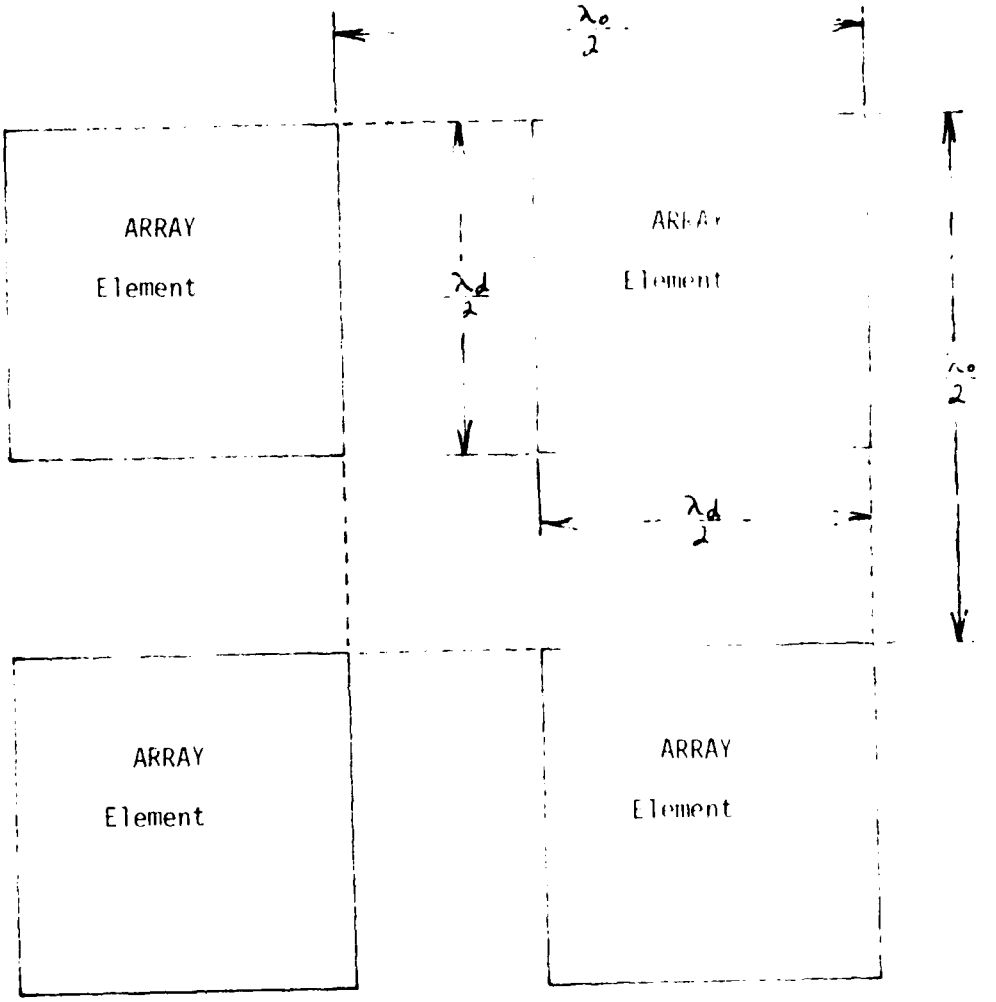


Figure 3. Inter-Element Surface Area

It has been shown that the minimum surface area requirement of $0.022\lambda d^2$ is associated with switched line phase bits. [1] A 3-bit device having switched line 180° and 90° bits and a loaded line 45° bit will consume an area of $0.075\ \lambda d^2$. Including three bias chokes at $0.33\ \lambda d^2$ each, the total phase shifter area requirement is $0.175\ \lambda d^2$ or half the available area. When the feed network and DC bias lines are added with adequate separation to prevent coupling, it is apparent that the design is impractical due to insufficient area.

This problem can be overcome, however, by replacing the half-wave elements with quarter-wave shorted elements. [2] Since the resonant or E-plane dimension is cut in half, the element area requirement is reduced from $0.25\ \lambda d^2$ to $0.125\ \lambda d^2$. Hence, the usable area from equation (1) is now $0.475\ \lambda d^2$. This 36% increase in surface area is sufficient to implement the monolithic hybrid design on teflon-fiberglass material.

The disadvantage of the quarter-wave element tradeoff is the added fabrication complexity compared to a full size element. As shown in Figure 1, one edge of the quarter wave element uses 14 plated through holes (PTH) to approximate a continuous short circuit. To fabricate the PTH's, two additional processing steps are required: drilling or punching and electro-plating. The associated tooling, labor and potential lower yields have the disadvantage of higher fabrication costs.

In terms of performance the quarter-wave element offers improved beamwidth and equivalent bandwidth with respect to the standard half-wave element. The E and H plane patterns of a quarter-wave element are shown respectively in Figures 4 and 5. The E-plane half-power beamwidth (HPBW) is nearly 170° which is indicative of the single slot radiator. The H-plane HPBW is substantially narrower at 82° due to the half-wave dimension in this plane.

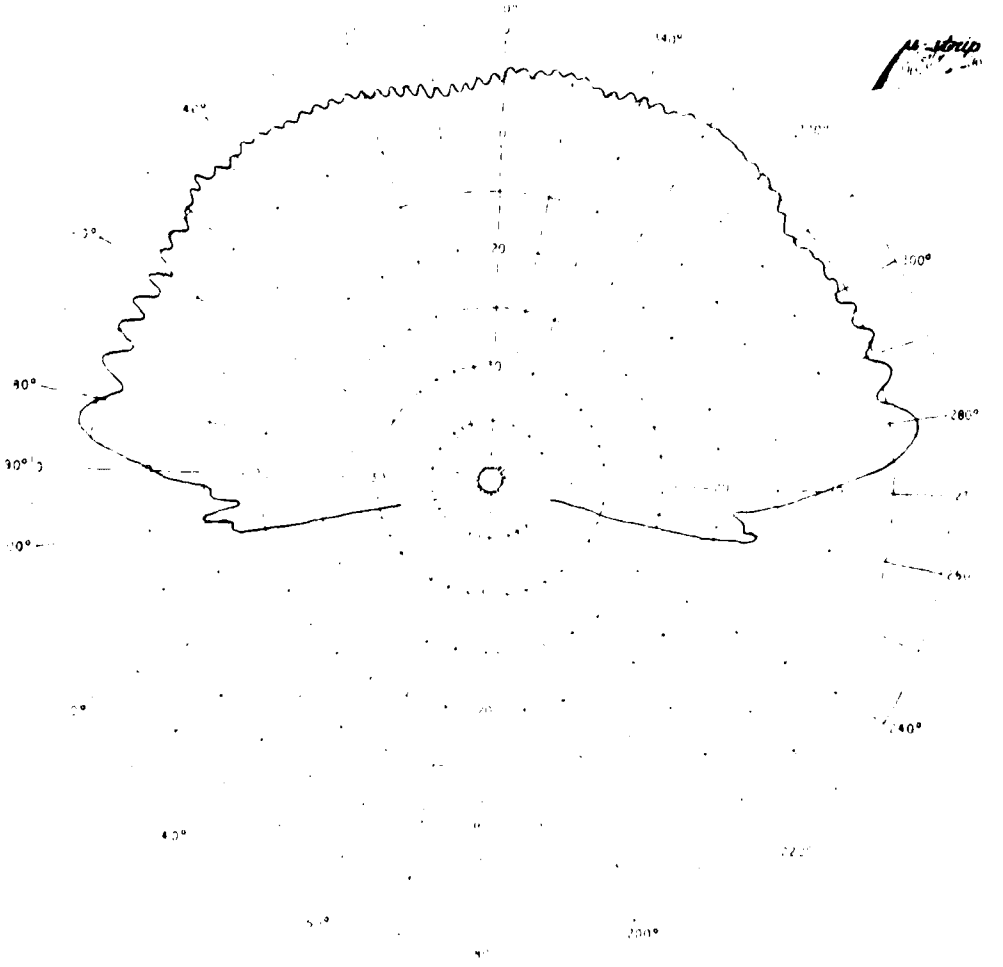


Figure 4. Quarter Wave Element E-Plane Pattern

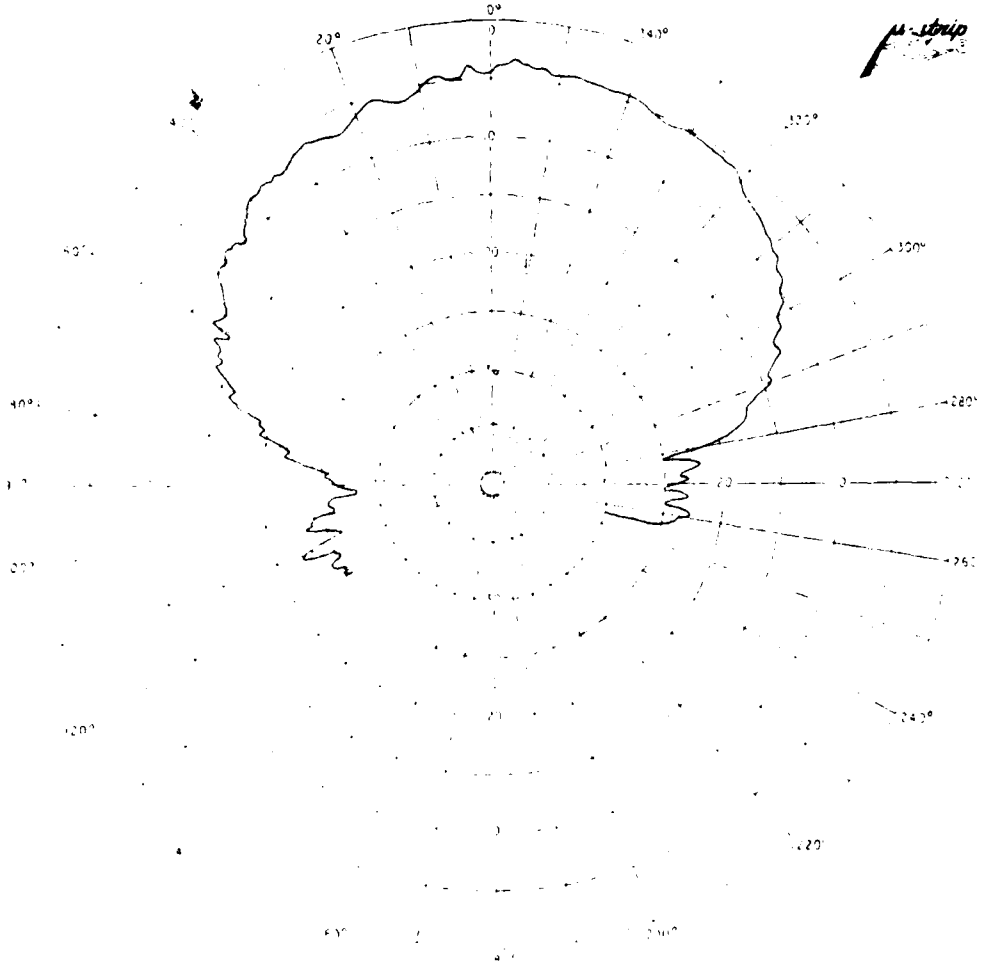


Figure 5. Quarter Wave Element H-Plane Pattern

In a 2-D scanning application this asymmetric element pattern will noticeably perturb the gain as the azimuth scan angle changes.

As mentioned earlier, the switched line phase shifter was an obvious choice in view of the area constraints. The disadvantage of this design, however, is the four diode per phase bit requirement. A typical 3-bit phase shifter with 180° and 90° switched line configurations and a 45° loaded line design has 10 diodes. In a large phased array with several thousand elements, DC power consumption is significant. Therefore phase shifter designs with only six diodes per element are preferred configurations.

A final observation on the monolithic/hybrid design is that the array surface is totally unprotected. For applications other than laboratory tests, a radome or protective cover is required to protect the hybrid components mounted on the aperture surface.

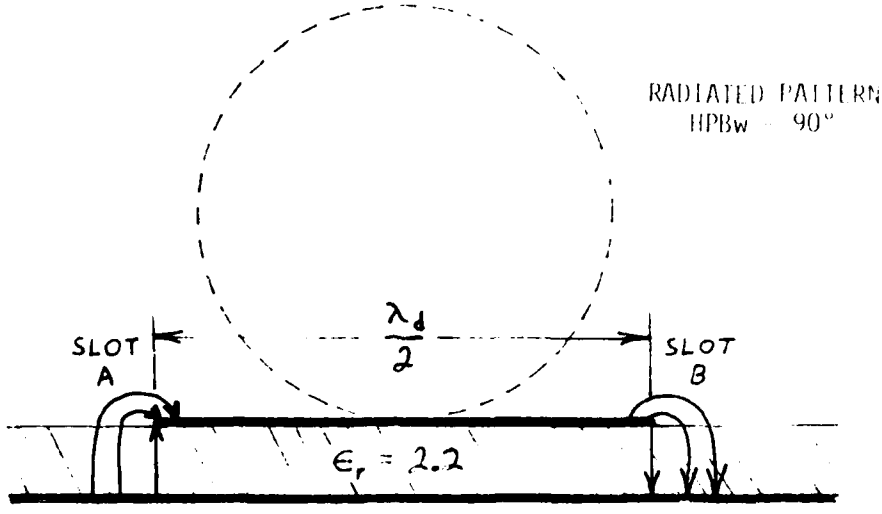
1.2.2 Monolithic/Hybrid High K Material

Many of the disadvantages associated with the monolithic/hybrid design on lower dielectric constant materials are overcome by simply increasing the dielectric constant. From equation (1) it is apparent that the available surface area increases with larger ε_r values. This is expected since the inter-element spacing, $\lambda o/2$, is independent of dielectric effects while the size of the microstrip element fabricated on the dielectric substrate decreases by $\sqrt{\varepsilon_r}$, allowing more area for the phase shifter and feed network. The advantage of only a slightly higher dielectric constant material is demonstrated by using quartz, ε_r = 3.78, as an example. From equation (1) the usable surface area is $0.146\lambda o^2$ and $0.184\lambda o^2$ for teflon-fiberglass and quartz respectively. The 26% increase in area on the quartz substrate

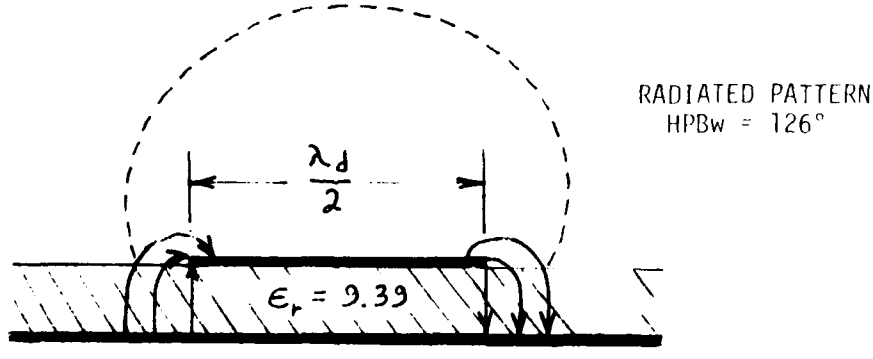
will allow the use of a standard half-wave element. This is important since the fabrication of PTMs in a rigid dielectric is substantially more complex and hence more costly compared to teflon-fiberglass materials. By eliminating the quarter-wave element requirement, the monolithic/hybrid approach on high dielectric constant materials is both simpler and lower in cost than its low dielectric counterpart.

Further increases in dielectric constant also result in design advantages. For example sapphire is an excellent microwave substrate material with $\varepsilon_r = 9.39$. From equation (1) the available surface area is $0.243\ \lambda_o^2$ ($2.28\lambda_d^2$) or 66% greater than the teflon-fiberglass baseline. As a result the larger, two-diode phase bits may be employed for the 180° and 90° phase bits and the implementation of a 3-bit, six-diode phase shifter becomes practical. The deletion of four diodes per element and the attendant reduction in drivers and decoding circuitry will cut the prime power consumption by 40%.

Another advantage of the high dielectric substrate material is the improved microstrip element performance. Both wider beamwidths and broader bandwidths have been demonstrated using sapphire substrates. Although the characteristics of this element will be presented in detail in Section 1.3, the theory behind the broader beamwidth is illustrated in Figure 6. In essence the microstrip element is a two slot radiator and the dielectric under the patch can be treated as a low impedance transmission line $\lambda/2$ long connecting slot A and slot B. The half-wavelength property of this transmission line is determined by the dielectric constant of the material, however, the radiated field is a function of the slot separation in terms of free-space wavelength. A typical element on teflon-fiberglass dielectric, $\varepsilon_r = 2.2$, is shown in Figure 6 (a) and has a HPBW of 90°. A comparable element of sapphire, $\varepsilon_r = 9.39$, is shown in Figure 6(b). The resonant dimensions or slot separation is reduced due to the



(a)



(b)

Figure 6. - Element Be width Comparison

higher dielectric constant resulting in a smaller aperture, hence broader beamwidth.

While high dielectric substrates offer many advantages for the monolithic/hybrid design, they are not without disadvantages as well. The most significant drawback is the higher microstrip feed network loss which is strictly a function of higher current densities in the conductor. For example, the conductor loss of a 100Ω microstrip transmission line on Duroid 5880 0.787 mm (.031 in) thick is 0.025 dB/cm. By way of comparison, the conductor loss of a 100Ω line on sapphire 0.381mm thick is 0.27 dB/cm or an order of magnitude greater. These are equivalent transmission lines since the dielectric thickness is .06λd in both cases. The width of the microstrip lines are 0.762mm and 0.051mm for Duroid and Sapphire respectively. The reason for the higher loss is current density related due to the 15 to 1 ratio of conductor areas.

Other disadvantages of the high K materials are that they are fragile and non-conformal. Conformal surfaces will have to be approximated by a number of flat pieces tangent to the surface. On large surfaces this may or may not be a problem since the antennas will consists of many subarrays. In general the availability of materials such as sapphire, as well as the thin film and photoetch processing equipment, will limit the subarray size to 8 x 8 elements or roughly 3.2 inches square.

1.2.3 Monolithic

A completely monolithic design maintains all of the advantages of the monolithic/hybrid approach while offering several significant improvements. At the present time it is a concept which will require extensive process development prior to implementation. However, it is considered here in view of the potential

benefits. We anticipate that the technology will be reduced to practice within the next 12 to 24 months.

Since the concept is the microwave equivalent of digital and low-frequency analog integrated circuits, the inherent advantages of very low cost, excellent repeatability and high reliability are expected to continue at frequencies well above X-band. These features are related to the cost-effective production techniques which involve very little labor. Devices and interconnections are fabricated in-situ with geometries specified and reproduced by the mask set.

Substrates amenable to monolithic fabrication must either be bulk semiconductor materials or have the capability of supporting the growth of a suitable semiconductor on their surfaces. Therefore, the viable candidates are limited to silicon on sapphire (SOS), gallium arsenide on sapphire and semi-insulating gallium arsenide (GaAs). Bulk silicon is unsatisfactory due to its poor loss tangent.

For the SOS material the active phase shifter elements will be PIN diodes. After diode fabrication the excess silicon would be removed so that the microwave circuitry can be deposited directly on the low-loss sapphire. The PIN diodes will remain as islands on the sapphire. PIN diodes fabricated in this manner, however, will be of low quality compared to the state-of-the-art since diffusion or implantation of dopants is restricted to the top surface.

For GaAs or GaAs on sapphire, the active phase shifter elements will be field effect transistor (FET) switches. Since these are predominantly planar structures, high quality devices could be fabricated by means of ion implantation on the top surface. Semi-insulating GaAs is an acceptable substrate since its high resistivity of 10^8 ohm-cm results in a loss tangent of 1×10^{-4}

which is equivalent to alumina. The dielectric constant of GaAs is 12.6 so all the scaling benefits of the monolithic/hybrid approach on high K materials will be enhanced with this design.

A further benefit of the monolithic design is that other active RF or digital devices may be incorporated at little or no cost increase. For example, amplifiers or mixers could be fabricated in-situ at each element at the same time as the active phase shifter devices. Similarly, digital control and logic circuitry and/or a distributed microprocessor could be included monolithically for each subarray. Although this will be more costly due to the additional mask and processing complexity, it is a far more cost-effective approach then the discrete component equivalent.

1.2.4 Multi-layer

The multi-layer approach is an appropriate extension of the monolithic/hybrid approach on low K dielectrics. It conveniently doubles the usable surface area by configuring the feed network and phase shifters beneath the array aperture. In doing so, full size half-wave elements may be used in the array along with the preferred six diode phase shifter configuration.

Perhaps the most significant advantage of this approach is that the active phase shifter elements are afforded greater protection from EMP and lightning. When these devices are located within the array beneath the element ground plane, analysis has shown that the PIN diodes and control electronics will survive these threats. [3]

Although this design eliminates the RF component crowding problem, it substantially complicates the hardware fabrication and mechanical assembly. Specifically, vertical interconnects must be installed between the monolithic phase shifter and radiating element layers. For example, in an 8 x 8 element subarray, the

precise registration of 64 holes will be required to assure a uniform characteristic impedance at 15 GHz. The impact of adding a second layer with its accompanying assembly problems is a significant cost increase over alternative designs.

In addition the multi-layer approach requires special mounting considerations. Since the two layers are mounted groundplane to groundplane, the phase shifter and feed network circuitry are exposed and must be isolated from the mounting surface. In the case of microstrip lines, an air gap of at least four substrate thicknesses is preferred. This standoff requirement can be avoided by using stripline but the increase in material cost and weight is substantial.

1.2.5 Modular

The modular approach is another convenient way of increasing the usable surface area by employing both high and low dielectic constant materials. In this design both the half-wave radiating elements and the feed networks are fabricated on teflon-fiberglass material to achieve closely matched E and H plane beamwidths and a low loss corporate feed. On the other hand, phase shifter circuits are produced on a high K material using hybrid circuit techniques in order to reduce size and costs. Assembly consists of integrating these pieces together.

The concept of removing low K material and inserting the high K substrate to retain a single layer is dismissed immediately on the basis of impedance matching. The degree of difficulty associated with maintaining a constant impedance level and a continuous groundplane across this interface makes the insert concept impractical.

The alternative then is to make the high dielectric material a lower layer in a multi-layer structure. Unfortunately, this has the same disadvantages as the multi-layer approach with additional complexity. Interconnect holes must also be drilled through the hard high K material as well as the teflon-fiberglass. Due to the fragile nature of the ceramic substrates, the fabrication and assembly of the modular/multi-layer array will be more expensive than the basic multi-layer concept previously described. Furthermore, the rigidity of the high dielectic material will severely restrict the conformal properties of the array.

1.3 Element Design

Since microstrip radiators on high dielectric constant materials are essential to the monolithic and monolithic/hybrid designs, an experimental evaluation was conducted during the analysis phase to establish performance levels. The dielectric materials included quartz, alumina and sapphire. Due to the exploratory nature of these designs, resonant frequencies close to 15 GHz were acceptable.

As a starting point, a 15 GHz element shown in Figure 7, was fabricated on 0.031 inch Duroid 5880. The E and H plane patterns, Figures 8 and 9 respectively, are computer plots of the measured data. Since the element is square with each side at 0.252 inch, the HPBWs are roughly equal at 60°. An impedance plot for the same element is shown in Figure 10. The 2:1 VSWR bandwidth is 2.2% or 333 MHz.

The Duroid design was then appropriately scaled and fabricated on a 0.015 inch thick quartz substrate shown in the lower left corner of Figure 11. The E-plane, H-plane and VSWR data are presented in Figures 12, 13, and 14, respectively. The E-plane HPBW is approximately 108 and the 2:1 VSWR bandwidth is 1.5% or

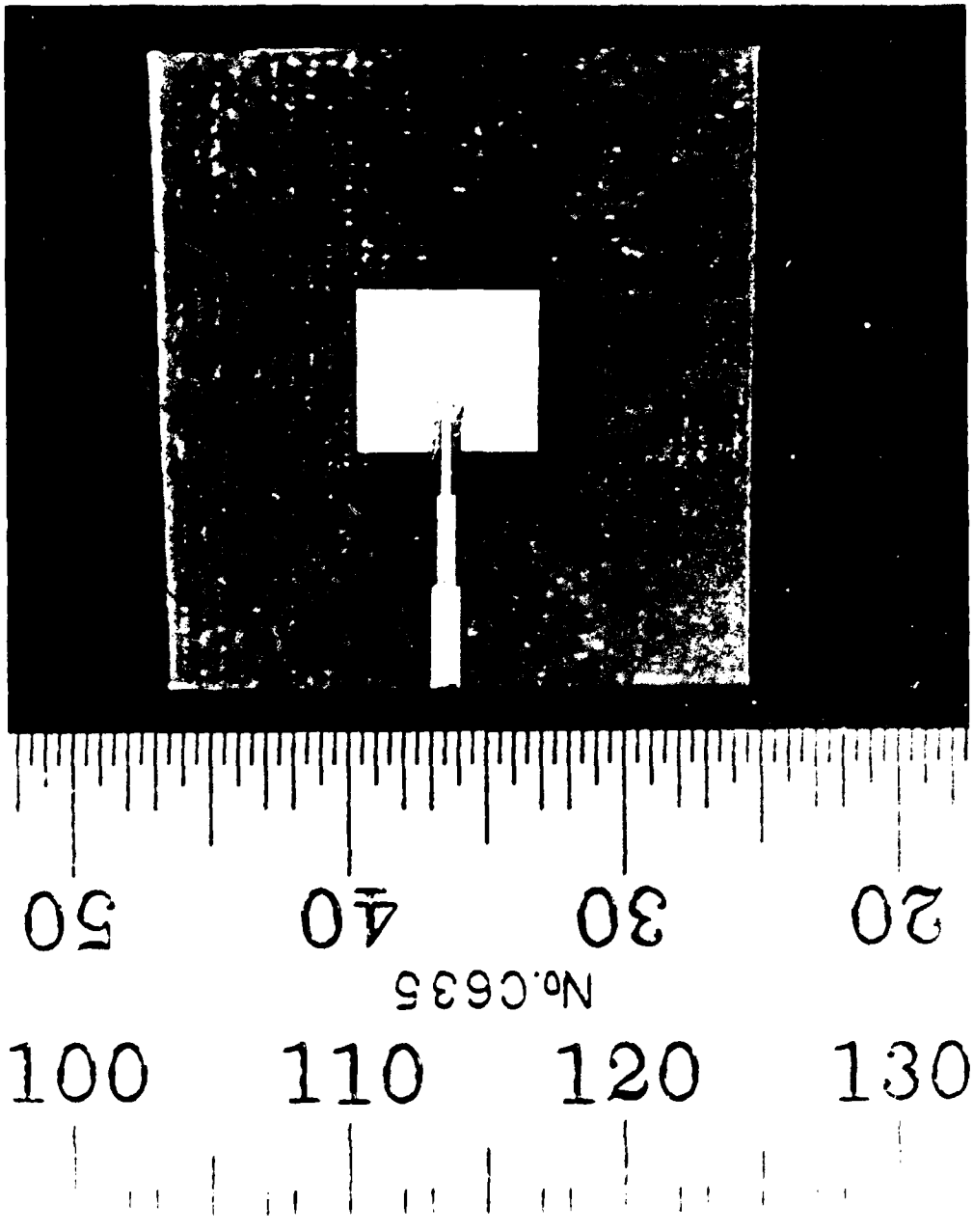


Figure 7. Teflon-Fiberglass Element

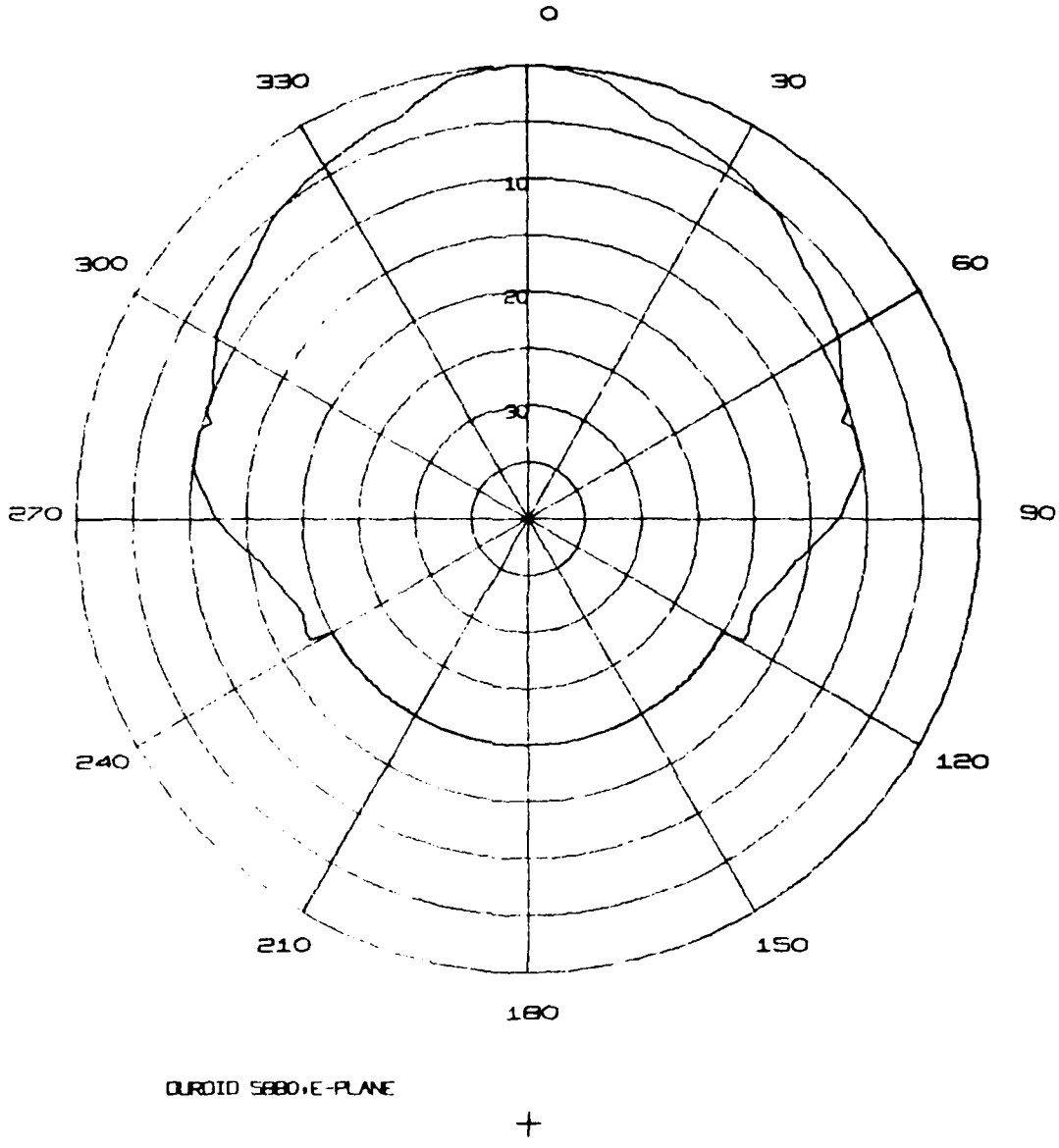


Figure 8. Teflon-Fiberglass Element E-Plane Pattern

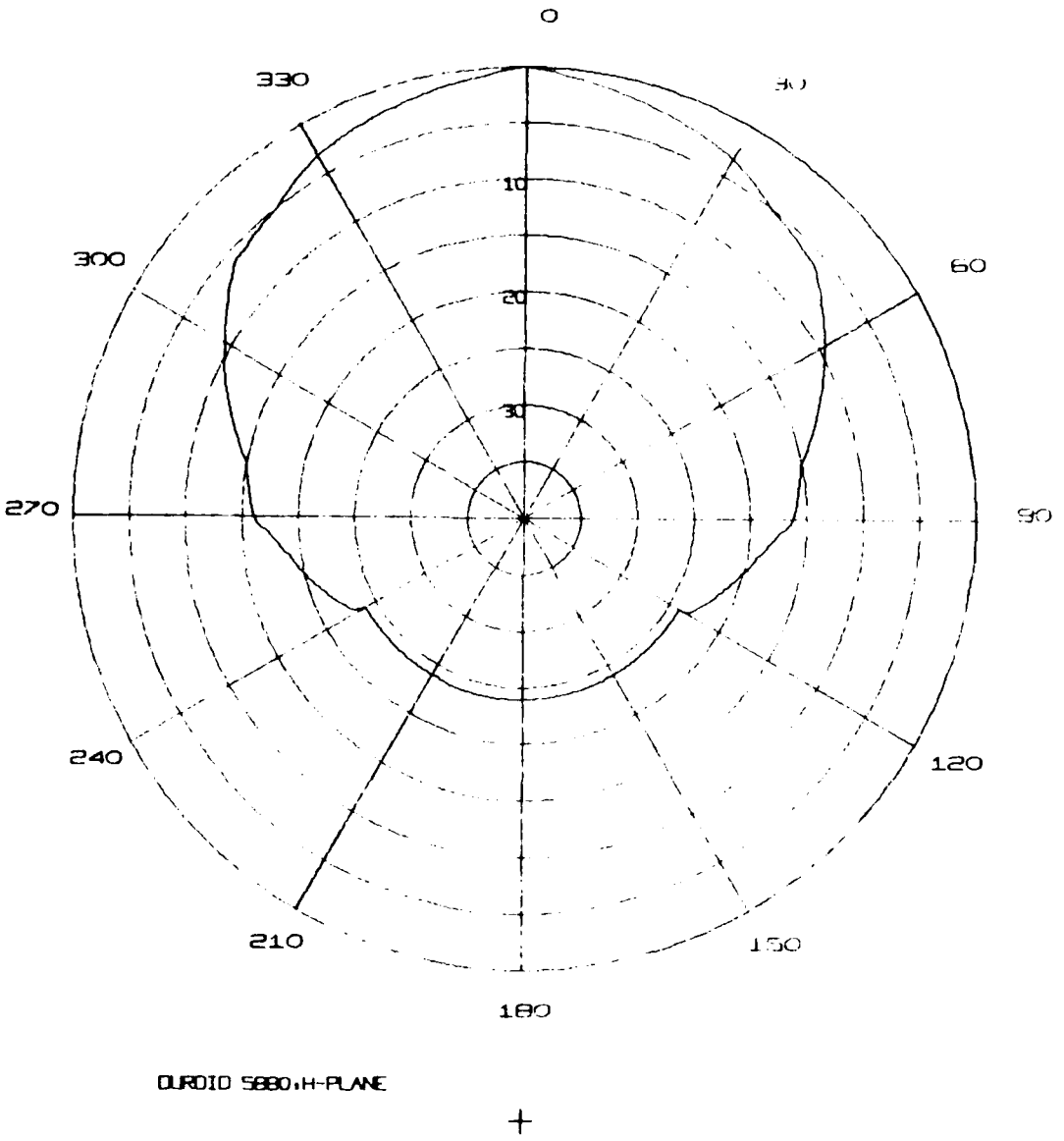


Figure 9. Teflon-Fiberglass Element H-Plane Pattern

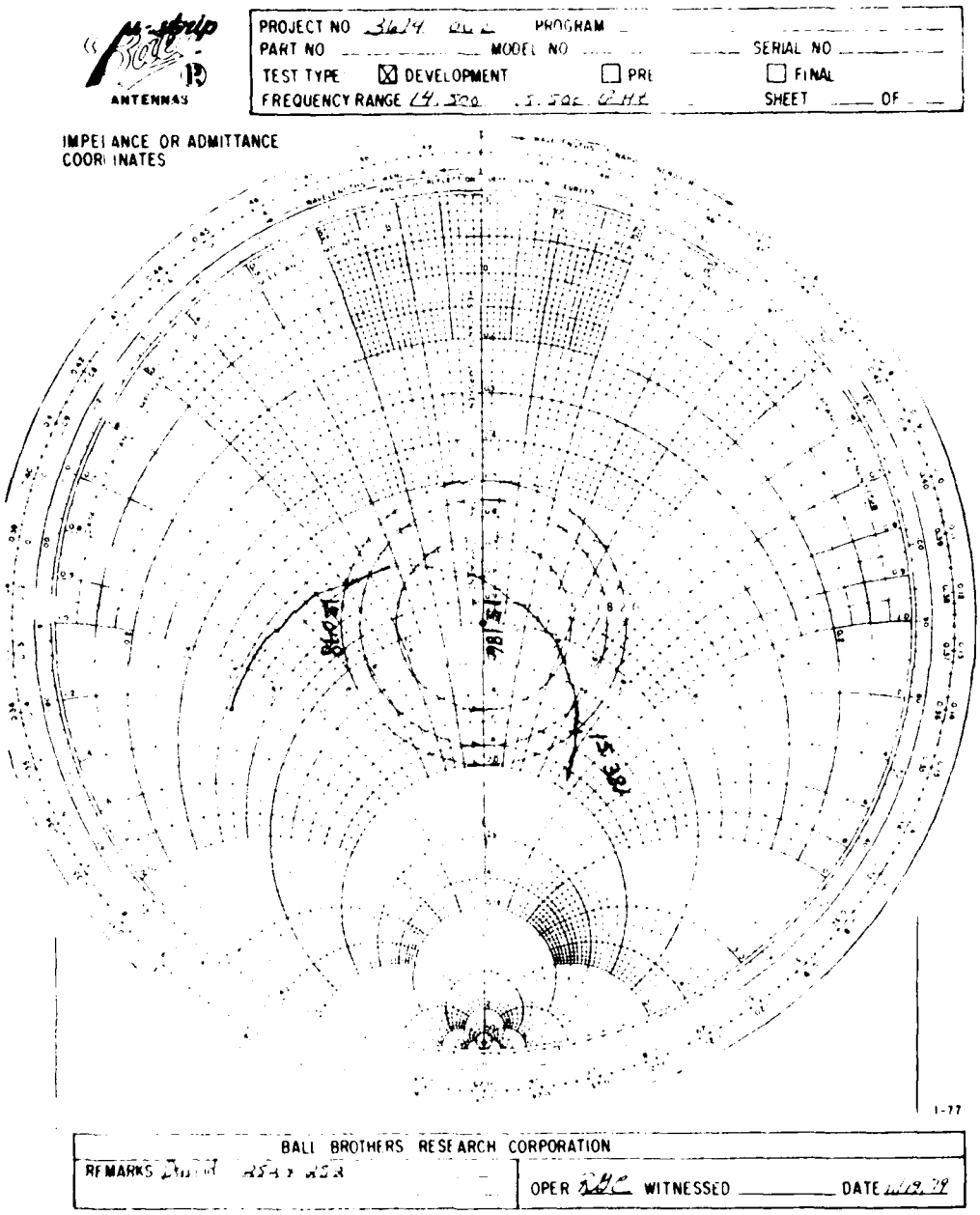
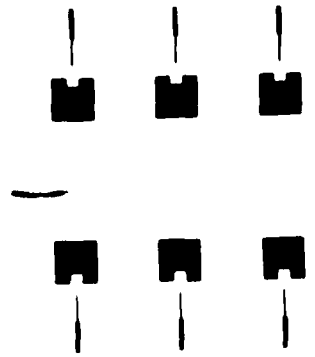


Figure 10. Teflon-Fiberglass Element Impedance Plot



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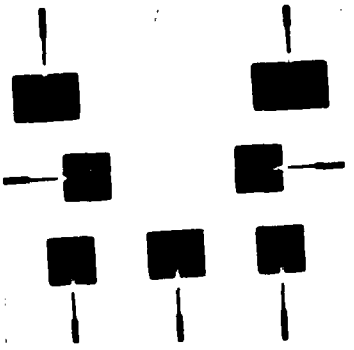

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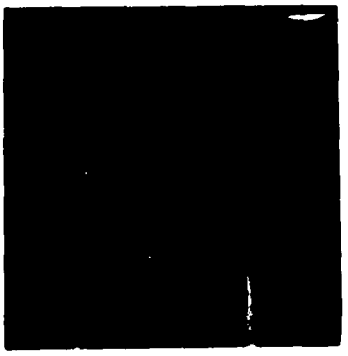


QUARTZ

SAPPHIRE

Figure 11. Microstrip Elements on Quartz, Alumina and Sapphire

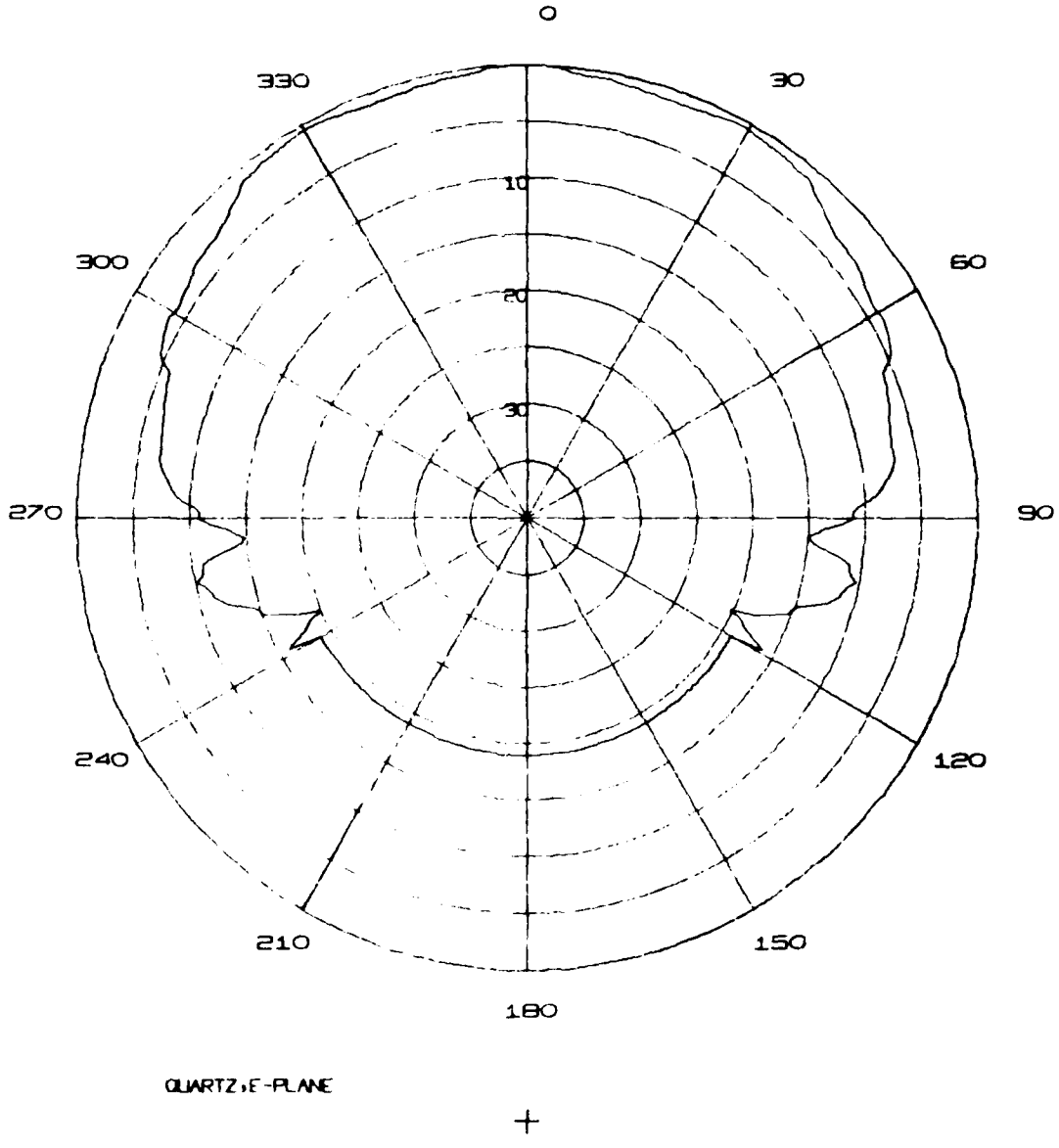


Figure 12. Quartz Element E-Plane Pattern

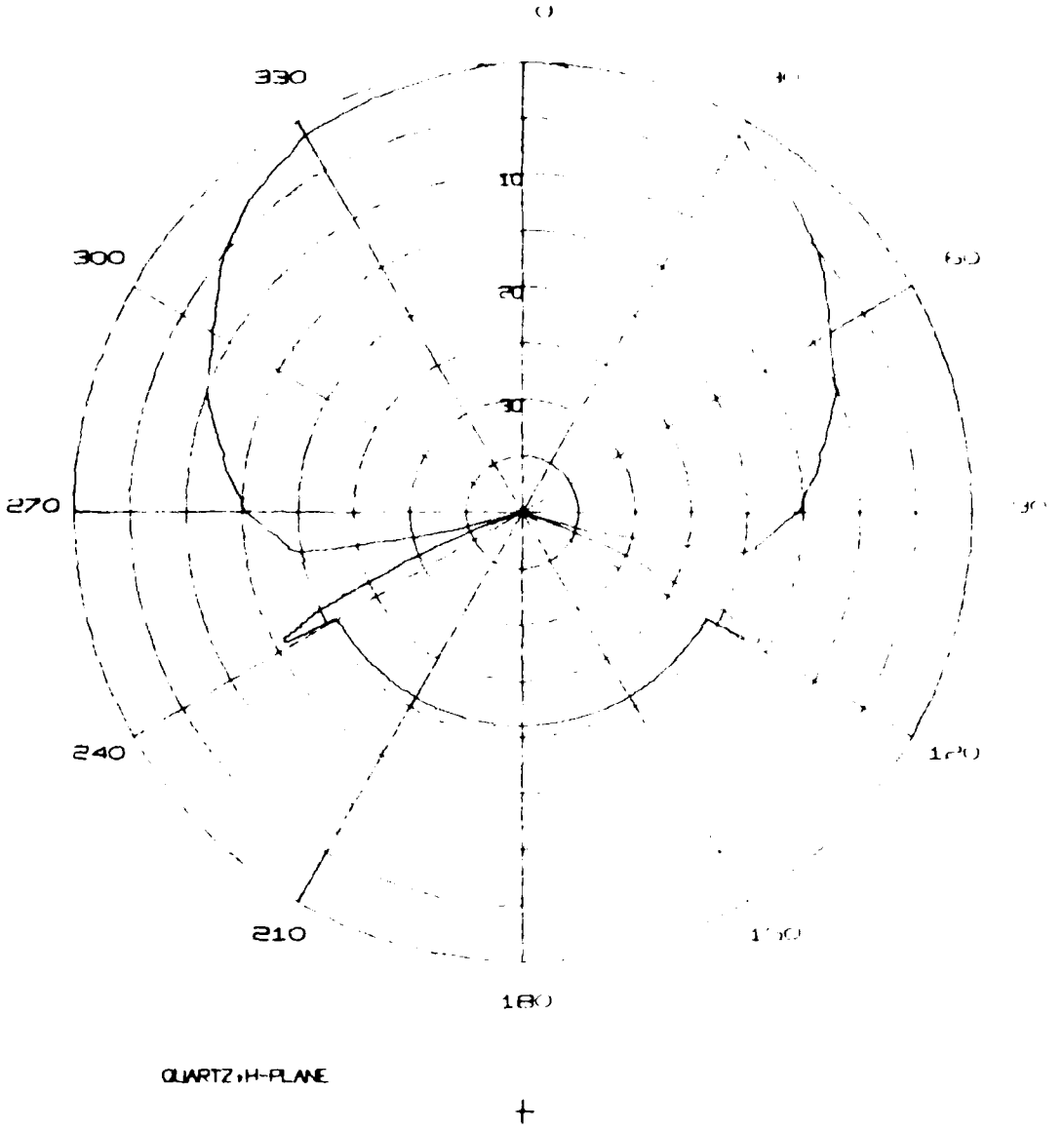


Figure 13. Quartz Element H Plane Pattern

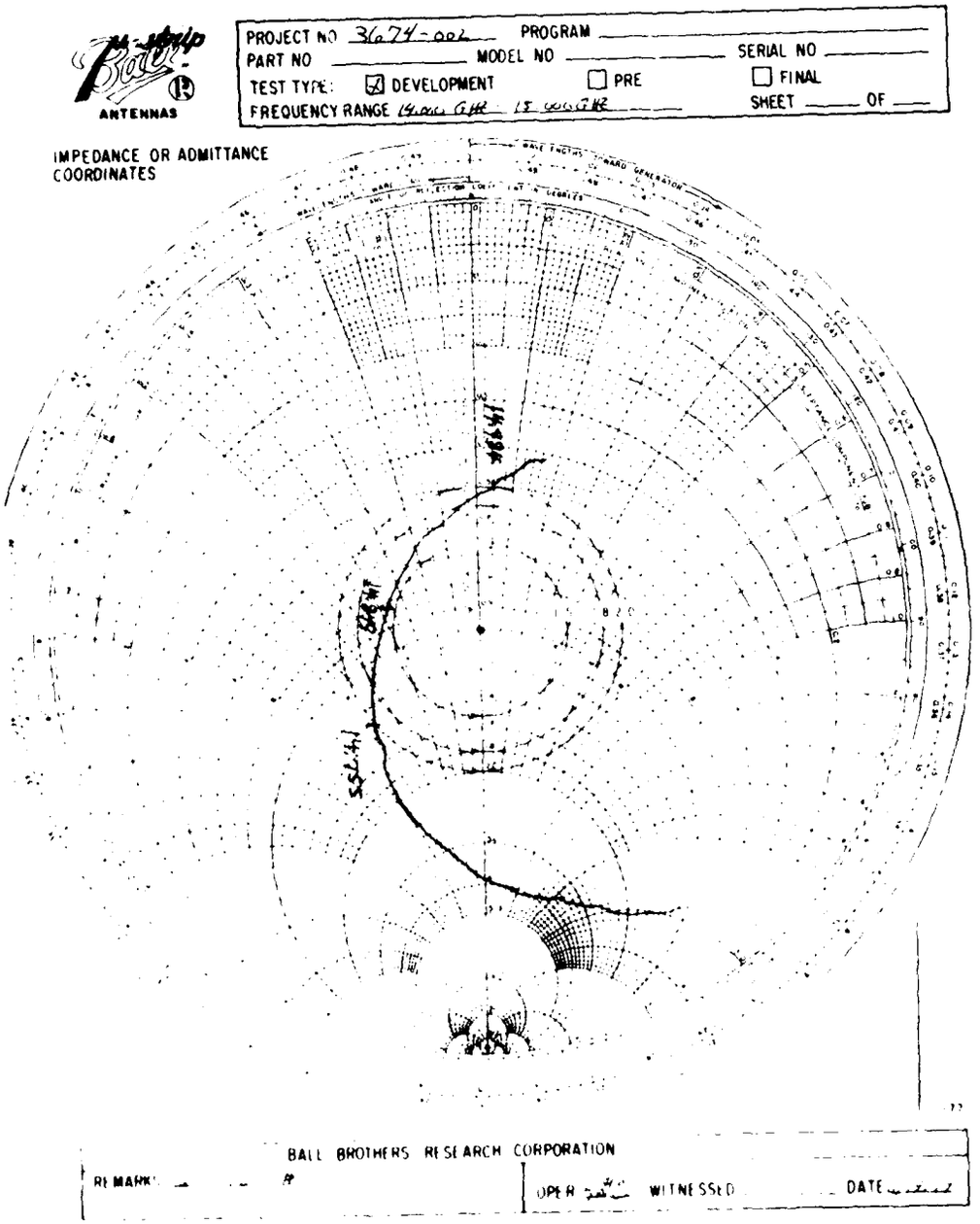


Figure 11. Quartz Element Impedance Plot

230 MHz. The reduced bandwidth is attributable to the substrate thickness. For direct scaling, the 0.031 inch or 0.058 λd thickness on Duroid should equate to a quartz thickness of 0.023 inch. The 0.015 inch dimension results in a λd of only 0.037, hence a narrower bandwidth is expected.

Figure 11 also shows a variety of microstrip radiators on alumina. The material was used as a cost effective substitute for sapphire during the early design stage since it has a dielectric constant of 9.8 compared to 9.39 for sapphire. Fully optimized elements were not completed on this material.

Due to the substantially higher dielectric constant of sapphire, square element configurations become impractical to implement. The slot conductance becomes so small that the input impedance exceeds several hundred ohms which is outside the range of practical microstrip lines. The solution, then, is to increase the slot conductance by extending the width of the slot. The result is a rectangular shaped element as shown in Figure 15 with a useful input impedance of roughly 100Ω.

The E and H plane patterns for the sapphire element are shown in Figures 16 and 17 respectively. As expected, the E-plane HPBW of 126° greatly exceeds the 60° value associated with the Duroid element. On the other hand, the H-plane beamwidth is 74° due to the 0.9λd dimension in this plane.

Perhaps the most striking feature of the sapphire element is the measured 2:1 VSWR bandwidth of 9.5% which is substantially greater than the typical 1-3% bandwidth associated with designs on lower dielectric materials. A VSWR plot of the element is shown in Figure 18.

The resonant frequency is 14.16 GHz and the 2:1 VSWR points are 15.14 and 13.8 GHz for a 1.34 GHz bandwidth. Although this

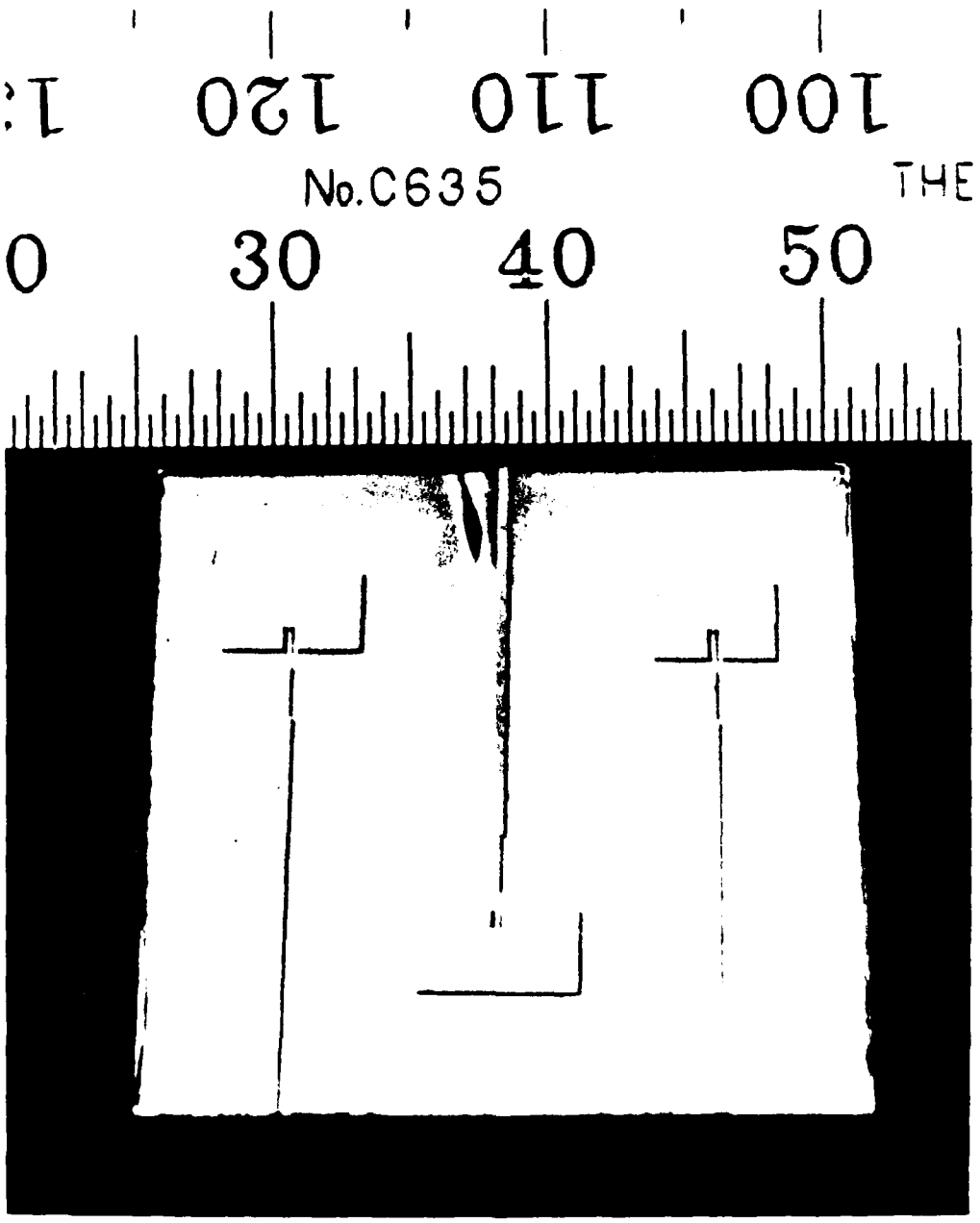


Figure 15. Sapphire Elements

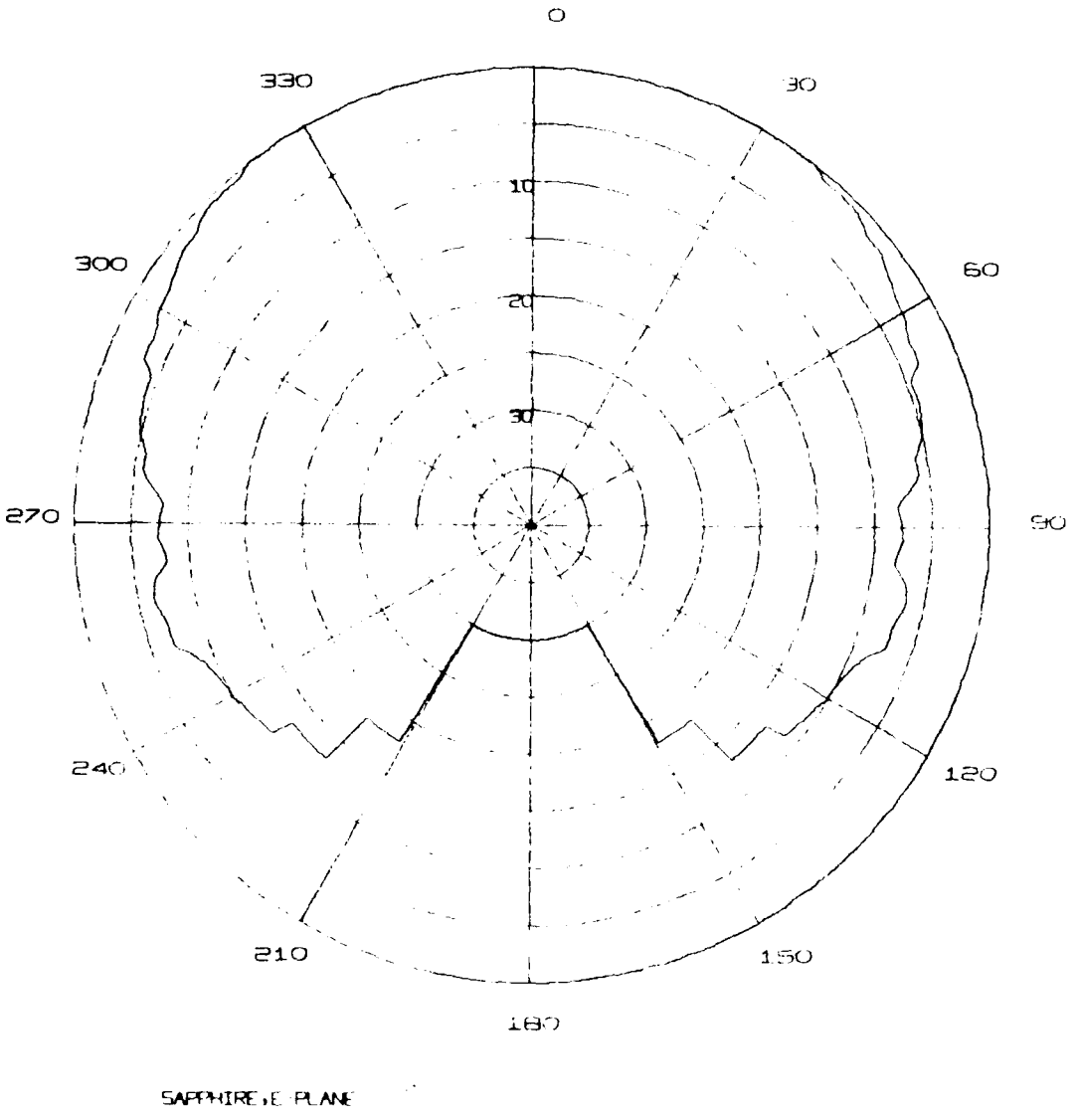


Figure 16. Sapphire Element E-Plane Pattern

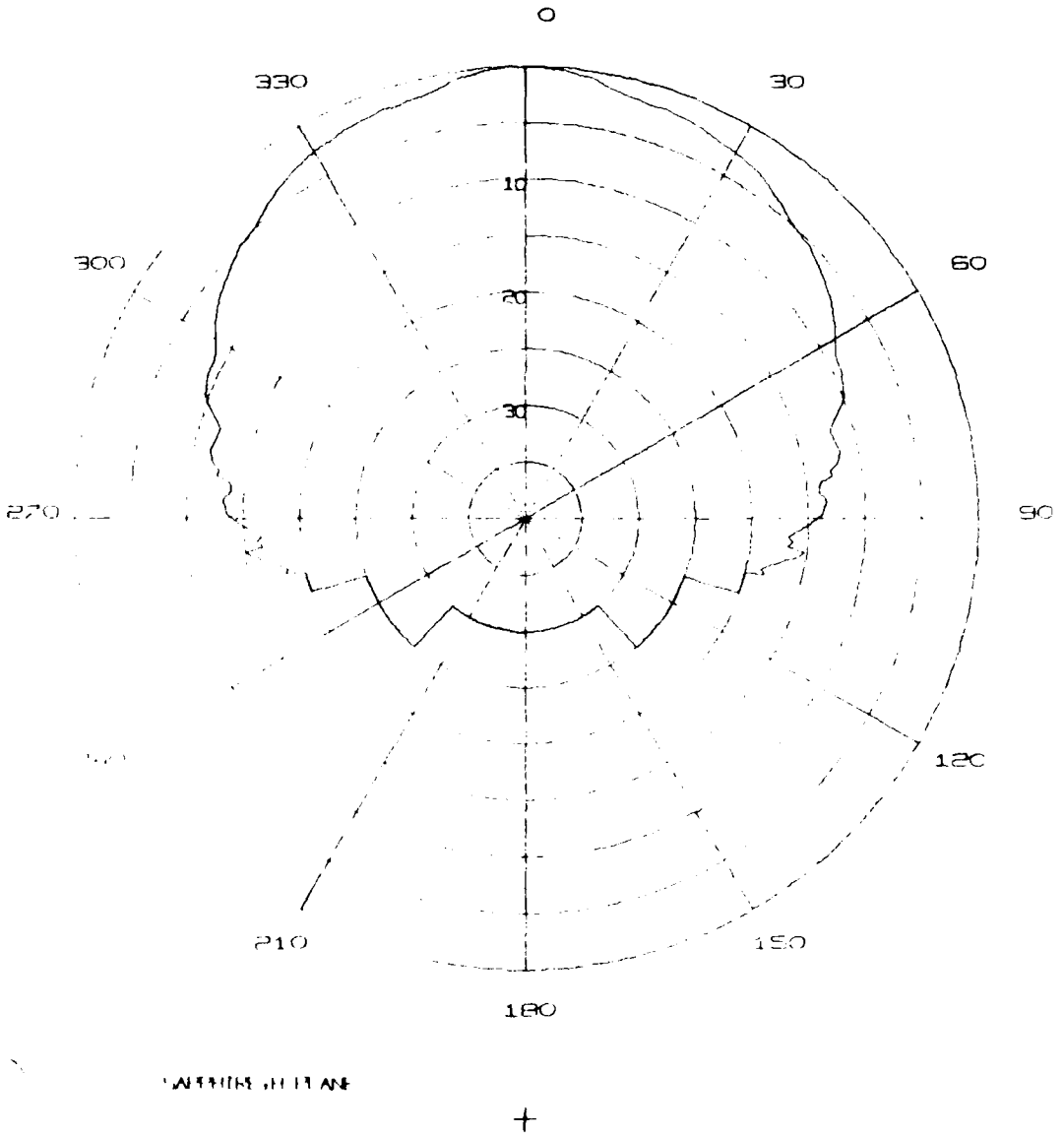


Figure 17. Sapphire Element H-Plane Pattern

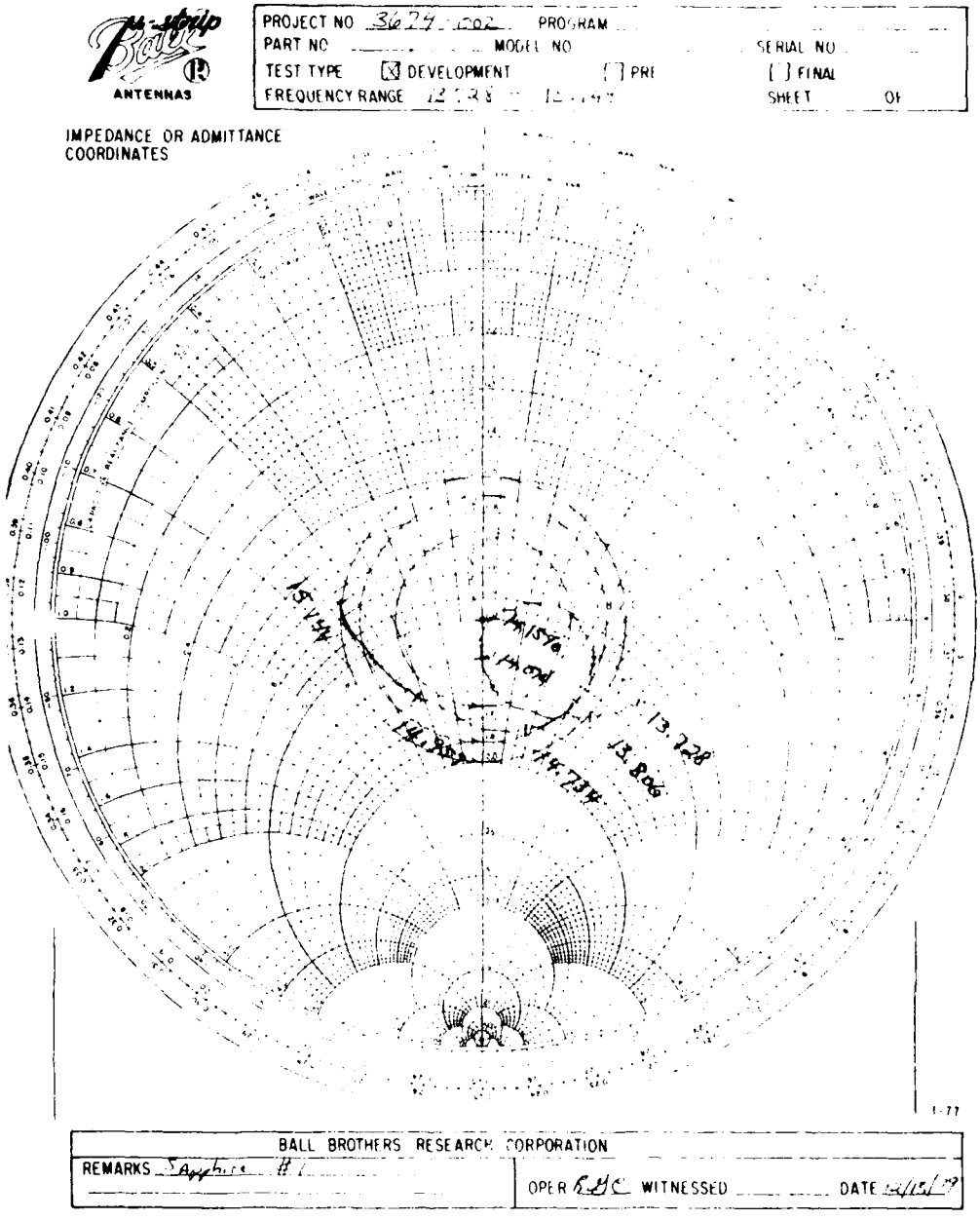


Figure 18. Sapphire E1 ... ent Impedance Plot

measured data is accurate and has been reproduced on numerous occasions it is somewhat overstated. An analytical assessment based on Derneryd's paper [4] yields a 6% 2:1 VSWR figure.

As an effort to reconcile the measured 9.5% and the calculated 6% bandwidth figures for the sapphire element, it is worthwhile to re-examine the measured data. The VSWR is measured with respect to the input port and does not include the loss of the 1.8 cm long transmission line between the input connector and the radiating element. This attenuation will "mask" the true VSWR, making it appear better than it actually is at the input connector. The theoretical loss of the transmission line consisting of 1.5 cm of 50Ω line and 0.2 cm of 100Ω line is 0.3 dB. This means that the 2:1 VSWR bandwidth of the radiating element corresponds to the 1.9:1 VSWR bandwidth at the input connector. A close examination of Figure 18 shows that the 1.9:1 VSWR bandwidth is 90 MHz less than the 2:1 bandwidth or 1.25 GHz. The true 2:1 VSWR bandwidth is 8.8% which is somewhat closer to the calculated value of 6%. The remaining 2.8% discrepancy is attributed to the increased width-to-length ratio compared to conventional designs. This design is not employed with low dielectric constant materials since λd and λo are not substantially different. Therefore, elements $0.9\lambda d$ wide will interfere with one another when spaced $\lambda o/2$ apart in an array lattice.

Since all of the elements are specifically intended for phased array applications, the individual element gains are secondary to beamwidth and bandwidth considerations. In the absence of quantitative gain measurements element efficiencies were verified by integration of the far-field patterns and found to exceed 95% in all cases. This was expected due to the good impedance match and extremely low loss tangents of 2×10^{-5} for both quartz and sapphire.

1.4 Array Considerations

The microstrip radiators on teflon-fiberglass, quartz and sapphire were evaluated as array elements by computer calculation of the far-field patterns.

Since the resultant pattern is the product of the element pattern and the array factor, the effects of the element characteristics can be isolated by maintaining a constant array factor. This is accomplished conveniently by examining the candidate elements in the same array lattice and at identical beam steering angles.

Calculations were performed for 8 x 8 element arrays with 0.43λ matrix spacing to prevent grating lobes at large scan angles. The 8 x 8 array was selected since it represents an optimum building block for larger high-gain antennas. The next convenient increment in size is 16 x 16 elements which is roughly 6 inches by 6 inches square at 15 GHz. For practical reasons this size is too large.

The availability of high dielectric materials (including quartz and sapphire) is extremely limited in size, not to mention expense. In addition, 6 inches by 6 inches is prohibitively large for most thin film processing equipment required for accurate pattern resolution at this frequency, regardless of dielectric material. Calculations also indicate that the losses in a microstrip feed network for 256-way power division will severely impact the overall efficiency.

On the other hand, the obvious smaller size is a 4 x 4 element building block which is too small. A high gain array would consist of many subarrays and the low loss feed network to the subarray level would require extra power division levels. Both

of these factors will reduce the cost effectiveness of high gain antennas.

Digital phase shifters were selected in view of their compatability with digital beam steering controllers and the planar construction techniques being investigated. Again, practical considerations dictated the use of 3-bit phase shifters. Less than 3-bits results in unacceptable, high quantization sidelobe levels. Conversely, 4-bit phase shifters will lower quantization sidelobes while increasing insertion loss slightly. However, the major drawback of the 4-bit device in conformal array applications is the additional surface area requirement which usually prevents its implementation.

The computed array patterns scanned 60° are shown in Figure 19, 20, 21 for the teflon-fiberglass, quartz and sapphire elements respectively. Assuming uniform illumination to achieve maximum gain, the first sidelobe levels are approximately -13.8dB. The pattern using the sapphire element is closest to the theoretical first sidelobe level since it has the broadest beamwidth. The difference between the sidelobe levels is directly proportional to individual element gains at that angle. For example, the sidelobes associated with the teflon-fiberglass element roll off much faster compared to the other elements since it radiates less energy at the far out angles.

At large scan angles, however, it is apparent that hemispherical coverage or broad beamwidth elements are preferred. The effect of the element pattern is illustrated in Figure 22 which shows the same 8-element array scanned to $\theta=60°$, $\phi=0°$. The teflon-fiberglass element is the dotted pattern and the sapphire element is solid. It is important to note the two major differences. First, the directivity is 0.3 dB less with the teflon-fiberglass element and second, the sidelobe levels are lower with the sapphire element. Both of these conditions are direct-

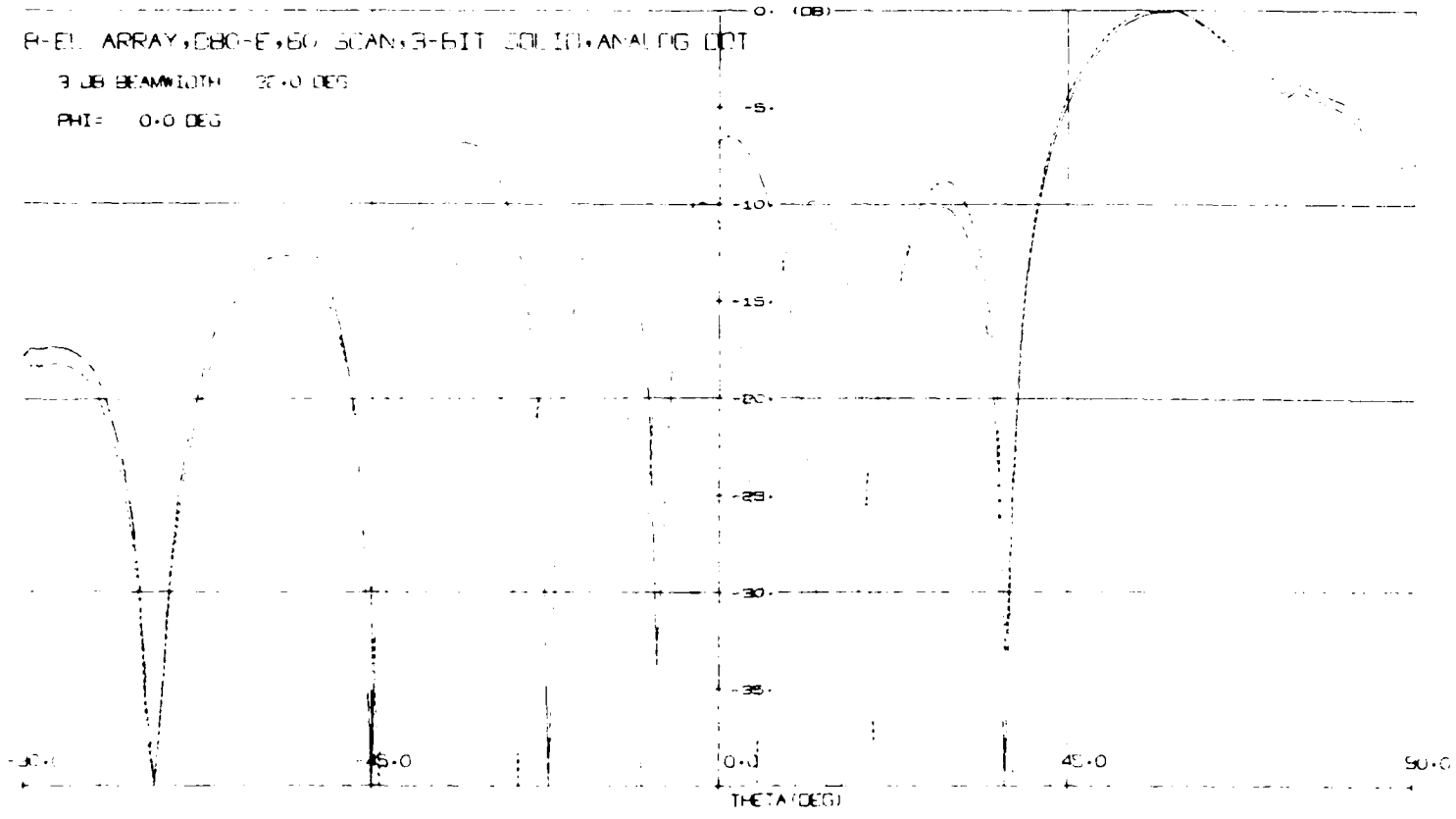


Figure 19. 8-Element Array Pattern With Teflon-Fiberglass Element

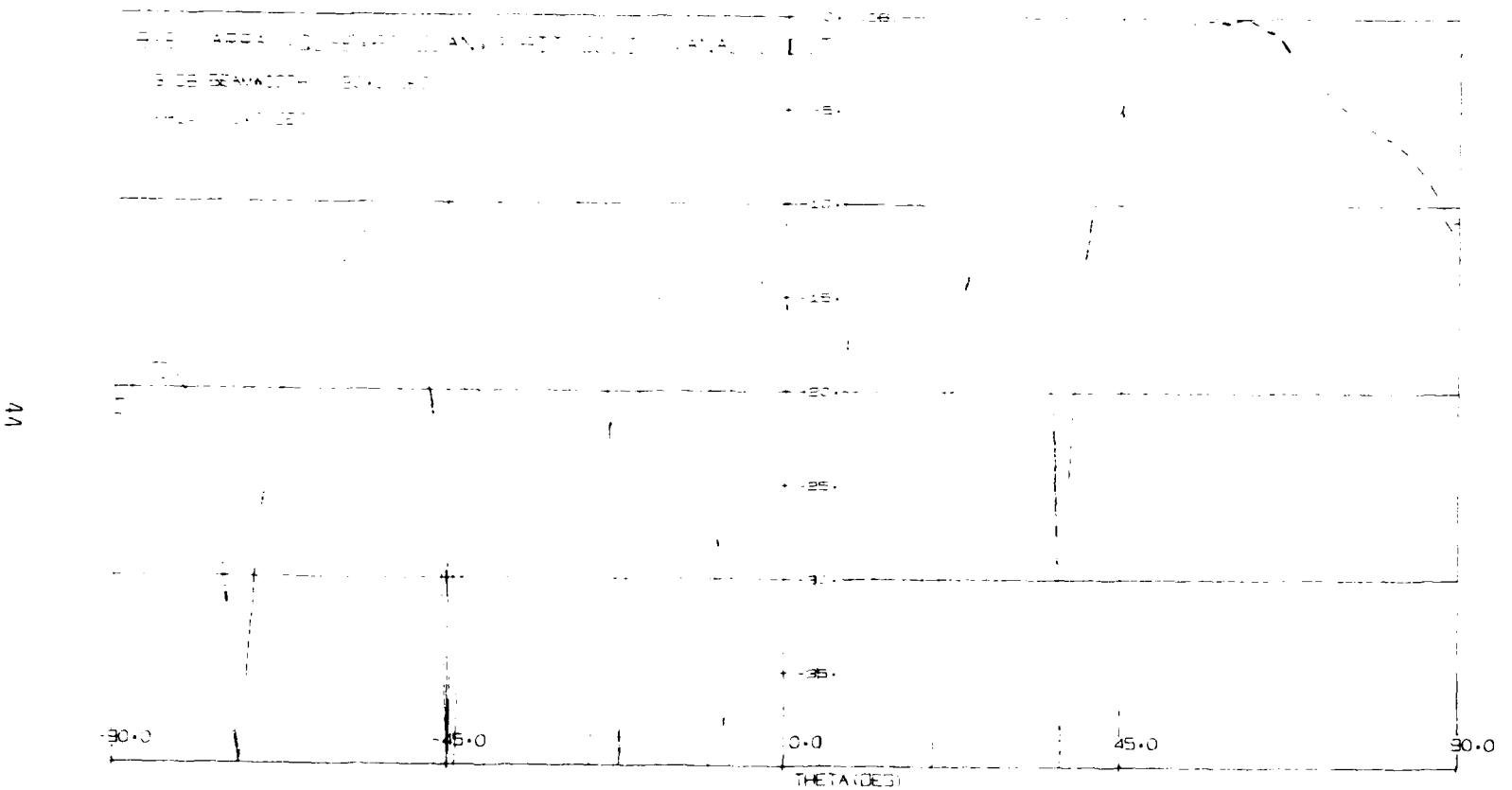


Figure 20. 8-Element Array Pattern With Quartz Element

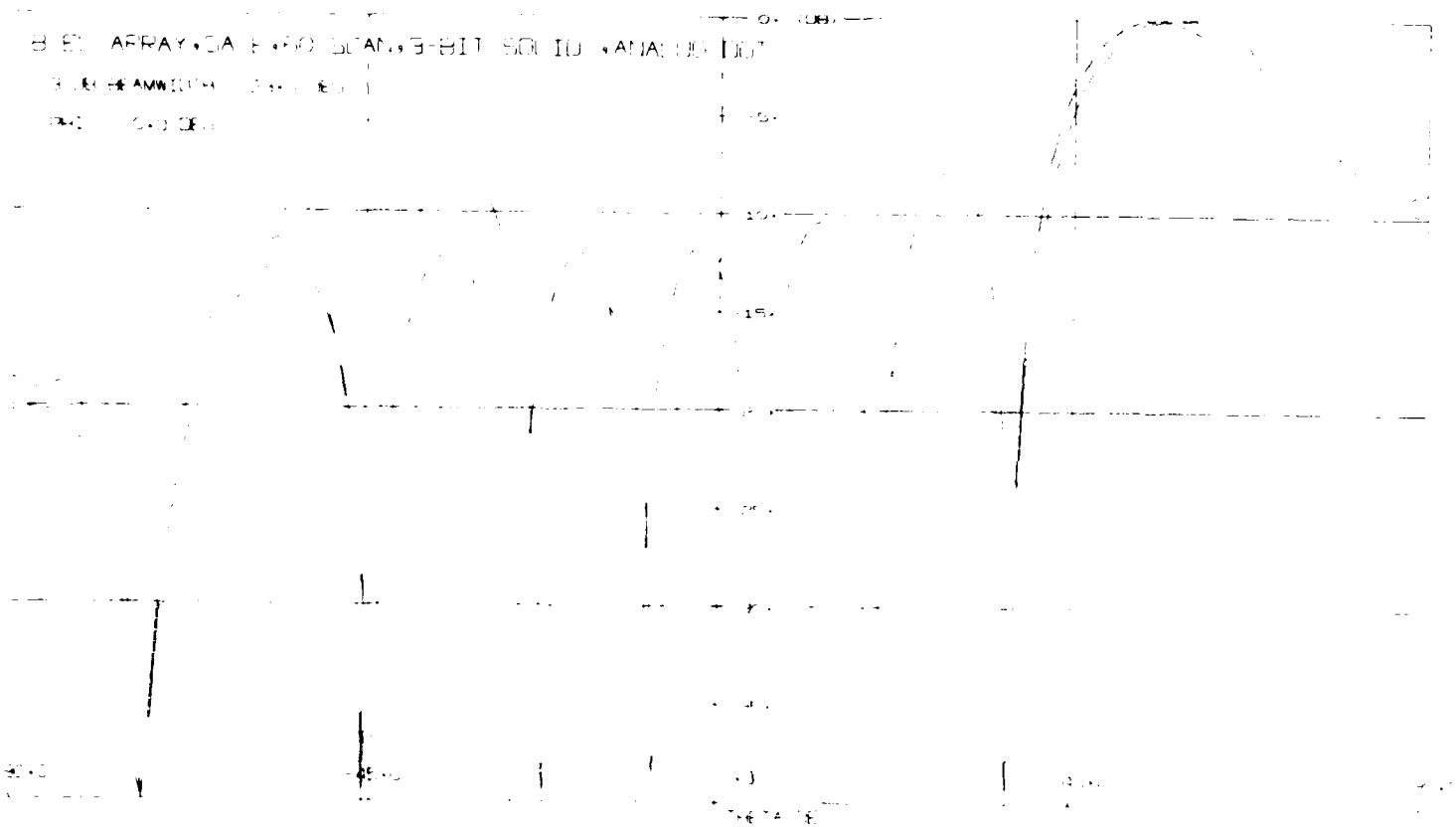


Figure 21. 8-Element Array Pattern with Sapphire Element

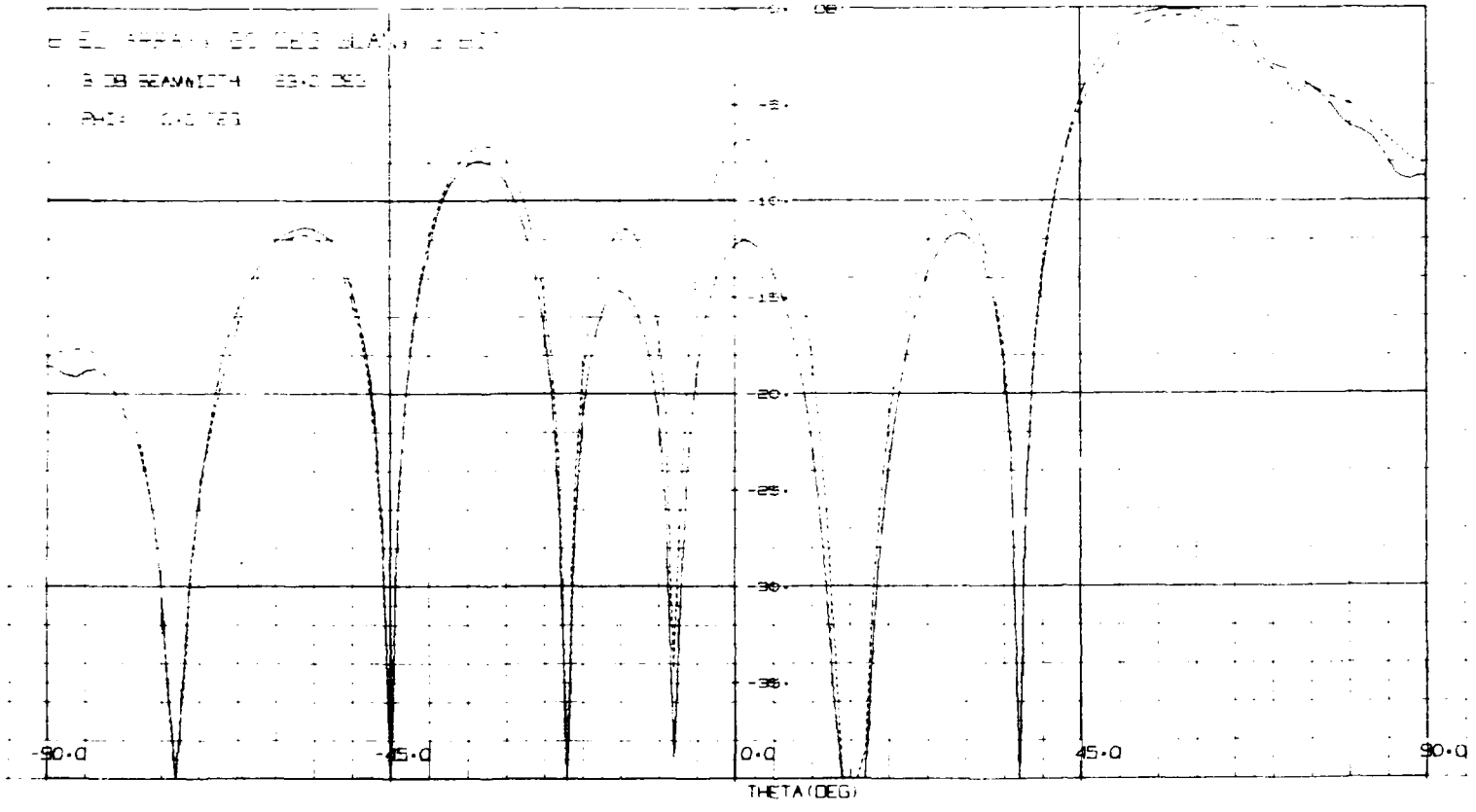


Figure 22. Effect Of Element Pattern On Array Pattern

ly attributable to the element characteristics. The more d rective teflon-fiberglass element radiates more energy at broadside than the sapphire element independent of array scan angle.

The conclusion, then, is that elements on high dielectric constant materials will improve phased array performance.

1.5 Phase Shifter Considerations

In conformal microstrip phased arrays, phase shifter tradeofts involve physical size, performance, prime power requirements and cost. For those designs which intersperse the phase shifters between the radiating elements, the surface area requirements are of primary importance, and often out rank performance. Since the objective of this program was to functionally implement the optimum array design, only conventional phase shifter circuits were investigated. The approach was to select different configurations of 180°, 90° and 45° phase bits to meet the specific requirements. For designs with severe space limitations, minimum area configurations were emphasized. Whenever a surplus of area was available, low loss designs were employed in as many bits as practical. The results of this procedure are summarized in Table 1.

A common concern involving all phase bit designs at 15 GHz is the availability of semiconductor control devices. The choice is limited to either PIN diodes or GaAs FET switches. Tuning diodes were dismissed due to poor performance in an identical application described in reference 5. The device selection is easy to make on the basis of cost. GaAs FET transistors for 15 GHz are roughly $100 a piece even when purchased as unpackaged chips. On the other hand the most expensive beam lead PIN diodes were only $15 each. Although the field effect transistors will offer a performance advantage in the application, the seven to one cost factor was not justified.

Table 1. Phase Shifter Configurations

PHASE SHIFTER CHARACTERISTICS	MONOLITHIC	MONOLITHIC/HYBRID		MULTI-LAYER	MODULAR
		D5880 & QU	SA	D5880/D5880	D5880/AL
180° BIT	FET SWITCHES	SWITCHED LINE	90° QUAD HYBRID	SWITCHED LINE	90° QUAD HYBRID
90° BIT	FET SWITCHES	SWITCHED LINE	90° QUAD HYBRID	SWITCHED LINE	90° QUAD HYBRID
45° BIT	FET SWITCHES	LOADED LINE	LOADED LINE	LOADED LINE	LOADED LINE
TOTAL DIODES	---	10	6	10	6
AVERAGE ARRAY POWER	---	16 W	10 W	16 W	10 W

For ease of fabrication a series [illegible] the active switching element in a [illegible] structure. The planar [illegible] served by installing the [illegible] the top conductor. Shunt [illegible] they require connection to the ground [illegible] substrate. This greatly complicates [illegible] costs and adds parasitic reactances. [illegible] configurations were avoided.

Performance in the series configuration [illegible] the following insertion loss and isolation equations:

Insertion loss (dB) = 20 log [illegible]

Isolation (dB) = 10 log [illegible]

To achieve low insertion loss and high isolation, it is apparent from the equations that diodes with both low series resistance (Rs) and low capacitance (C_T) are preferred. The best commercially available diodes have a R_s = 3 ohms and a [illegible]. Assuming a 50 ohm impedance environment, the theoretical insertion loss and isolation are 0.26 dB and 13 dB, respectively. Varying the impedance level will improve one value while degrading the other. Therefore, the above calculated values were used as the switching device loss figures in each of the phase bits. The balance of the loss in each phase bit is due to ohmic and mismatch losses. Using the procedures outlined by Garver [6], the total calculated loss for a 4 bit phase shifter on teflon-fiberglass was 2.1 dB which represents the minimum loss design. Unfortunately, the insertion loss advantage associated with the larger branch-line hybrid design was exceeded by the increased conductor losses on the higher dielectric constant substrate.

as a result, a net increase in insertion loss of 0.2 dB is expected between the monolithic/hybrid designs on Duroid 5880 and sapphire. The advantage, however, is in the reduced number of diodes, six instead of ten.

In addition to overall lower costs, the significance of this reduction is 40% less prime power consumption. In a 3-bit phase shifter with switched line 180° and 90° phase bits and a loaded line 45° bit, two of the four diodes in each of the two larger bits are forward biased in only four of the eight phase states, for an average number of "on" diodes per phase state of 3.

On the other hand, the 3-bit phase shifter having 180° and 90° bit diode switch type I designs and a loaded line 45° bit, each bit of which will be "on" in only half of the phase states. The average number of diodes per phase state in this design is only [illegible] of a forward bias current of 25 mA with a [illegible] the power dissipated per diode is roughly 0.025 watts. For a 4096 element array the average prime power [illegible] power supply inefficiencies and control [illegible] would be 10 watts. For the 10 diode phase [illegible] prime power requirement is roughly [illegible] system this 6 Watt difference [illegible] watts.

[illegible] of the monolithic phase shifter is [illegible] design concept is based on the [illegible] will be fabricated on semi- [illegible] design will permit the fabri- [illegible] with superior performance over PIN [illegible] however, due to the speculative status of this [illegible] phase shifter insertion loss of 2.2 [illegible] in Table [illegible].

1.6 Array Performance Estimates

A loss budget for each of the design concepts is presented in Table 2. This data is based on the individual component evaluations developed in the previous sections.

The 23 dBi directivity figure is calculated for a 8 x 8 element array with half-wavelength element spacing. Again, the value applies to all of the design concepts since the aperture size is identical with respect to λo. The gain is derived for each design concept by subtracting the projected system losses from the directivity.

The 95% element efficiency is implied for all of the designs by the 0.3 dB loss term. As mentioned in section 1.3 this performance level is achieved on the three basic substrate materials. Phase shifter losses vary slightly primarily due to the difference in transmission line loss per unit length.

This same factor explains the significant differences in the feed network loss figure. Higher current densities, hence higher losses, are associated with the thinner conductor widths on the high dielectric substrates. At the same time the feed network becomes longer in terms of λd for higher K substrates.

For the monolithic and monolithic/hybrid designs, an array mismatch loss of 0.5 dB was assumed to correspond to a 2:1 input VSWR level. This value was increased slightly to 0.6 dB for the multi-layer and modular designs to account for the vertical interconnections between the two boards.

The total system losses range between 3.5 and 4.8 dB for the monolithic/hybrid design on teflon-fiberglass and sapphire respectively. The corresponding gains and efficiencies are 19.5 dBi, η = 44.7% and 18.2 dBi, η = 33% for 8 x 8 element subarrays.

Table 2. Array Loss Budgets

PARAMETER	MONOLITHIC	MONOLITHIC/HYBRID			MULTI-LAYER	MODULAR
		D5880	QU	SA	D5880/D5880	D5880/AL
DIRECTIVITY (dBi)	23.0	23.0	23.0	23.0	23.0	23.0
ELEMENT	0.3	0.3	0.3	0.3	0.3	0.3
PHASE SHIFTER	2.2	2.1	2.2	2.3	2.1	2.3
FEED NETWORK	0.9	0.6	0.9	1.7	0.7	1.2
MISMATCH	0.5	0.5	0.5	0.5	0.6	0.6
TOTAL LOSSES (dB)	3.9	3.5	3.9	4.8	3.7	4.4
BROADSIDE GAIN (dBi)	19.1	19.5	19.1	18.2	19.3	18.6
EFFICIENCY	40.7%	44.7%	40.7%	33%	42.7%	36.3%

LOSS BUDGET FOR 8x8 ARRAY

1.7 Array Mechanical Details

Although RF performance is of primary importance in evaluating the candidate designs, the mechanical characteristics are essential considerations for a thorough tradeoff analysis. Computations concerning size and weight for each design concept for the basic 8x8 subarray building block are summarized in Table 3.

Since the aperture size is dictated by λ_0, the planar surface area is the same for all designs at 11 square inches. Therefore, the weights are determined by material thicknesses and densities.

The monolithic and monolithic/hybrid designs are single substrate structures of the thickness indicated. In the multilayer and modular designs, however, the thickness represents the overall dimension of the two substrates. The multi-layer design consists of an element layer on a 0.031 inch board and a feed network/phase shifter layer on a 0.020 inch substrate. Both layers are Duroid 5880 teflon-fiberglass material.

In the modular design the elements and feed network are on 0.031 inch teflon fiberglass, but the phase shifter modules are fabricated on alumina substrates 0.015 inch thick. Although the total surface area of the four high dielectric modules is only 40% of the aperture area, the overall thickness is the sum of the two layers or 0.046 inch.

It should be noted that the thickness dimension for both the multi-layer and modular designs does not include the air gap or standoff dimension. This spacing is required since the lower layers in both designs have the circuitry on the bottom as mentioned in section 1.2. This spacing requirement is typically four substrate thicknesses.

Table 3. Array Mechanical Details

	MONOLITHIC	MONOLITHIC/HYBRID			MULTI-LAYER	MODULAR
		D5880	QU	SA	D5880/D5880	D5880/AL
ARRAY THICKNESS (IN)	.015	.031	.024	.015	.051	.046
ARRAY WEIGHT (GM)	6.4	12	10	11	20	16

The array weights presented in Table 3 range between 6.5 and 20 grams per subarray. Compared to conventional antennas at lower frequencies this weight seems almost negligible. An array which would have a broadside gain of approximately 36 dBi and which would consist of 64 of the heaviest subarrays (20 gm each) would weigh less than 5 kg. Of this total maximum weight, the 64 subarrays only comprise 1.28 kg. The remaining 3.7 kg is array structure, fairing, radome and electronics. If monolithic subarrays were used with integrated electronics, a realistic overall weight of less than 3 kg is expected.

1.8 Cost Comparisons

A comparison of direct manufacturing costs for prototype quantities was also included as part of the analysis effort. Although the results presented in Table 4 are cost estimates, they are believed to be quite accurate.

Concurrent with this program, BASD was fabricating an 8x8 multilayer array on teflon-fiberglass material at 7.5 GHz. Since the hardware fabrication was for another RADC program, it provided a timely basis for the cost analysis in this study effort. These costs are summarized in the column labeled multi-layer, D5889/D5880. Except for two modifications these dollar values represent actual costs. First, the antenna material costs which include board material and PIN diodes were scaled to reflect the one-fourth substrate area requirement associated with the frequency doubling. Second, the assembly labor for PIN diode installation was recomputed using the fastest production rates to eliminate "learning curve" inefficiencies.

In Table 4 the antenna materials category includes the substrate material, PIN diodes and blocking capacitors. The costs associated with the six fabrication techniques primarily reflect the

Table 4. Direct Manufacturing Costs x $1,000

	MONOLITHIC	MONOLITHIC/HYBRID			MULTI-LAYER	MODULAR
		D5880	QU	SA	D5880/D5880	D5880/AL
MATERIALS						
ANTENNA	0.2	5.0	5.1	3.25	5.0	3.0
DIGITAL CIR	---	8.0	8.0	4.8	8.0	4.8
FABRICATION	0.05	0.25	0.05	0.05	0.2	0.3
ASSEMBLY	---	0.8	0.8	0.48	1.6	1.8
TOTAL COSTS	0.25	14.05	13.95	8.58	14.8	9.9
RELATIVE COSTS	1.0	56.0	56.0	34.0	59.0	40.0

difference between the 10 diode and 6 diode phase shifter circuits. This difference is also apparent in the digital circuitry material costs which include all of the electronic control circuitry for the phase shifters. These components are essential for an operating system and the cost is basically the same whether the digital hardware is located at the antenna or external to it.

For the monolithic design, however, the total materials cost is $200 for the system. RF and digital components will be fabricated in-situ and therefore cannot be costed as discrete components. Instead, the fabrication cost includes all the processing steps to create the radiating elements, feed network, transmission lines, phase shifter components, digital integrated circuits and dc distribution network. In general the capacity of the semiconductor processing equipment greatly exceeds one wafer. Therefore, fabrication costs are actually process cycle costs independent of the number of wafers. Assuming that equipment capacity is 100 wafers, two man-months of highly skilled labor can be amortized so that the fabrication cost per unit is roughly 50 dollars.

The fabrication costs for the other design concepts refer to processing of the circuit boards. The monolithic/hybrid designs on quartz and sapphire are lowest since one photolithographic procedure is required. Both the multi-layer and modular approaches involve more than one photoetch process with extra punched or drilled holes between the various layers which substantially increases the cost. The monolithic/hybrid approach on Duroid is equally expensive due to plated through hole requirements for each element.

The assembly costs are indicative of the degree of difficulty involved. The modular approach is most complex because of the vertical interconnects between the element feed network layer

and the 16 phase shifter modules. These are also required in the multi-layer design but the cost is somewhat lower since only one phase shifter substrate is required.

The monolithic/hybrid designs are least expensive since only PIN diode and blocking capacitor installations are required. These designs do not require multiple layer interconnects. The monolithic/hybrid design on sapphire is less expensive due to the 6 diode phase shifter.

The total cost for each design is tabulated at the bottom of the table. For comparison the relative costs are computed by normalizing each total with respect to the minimum which is the monolithic design at $250 per subarray. The next lowest cost design is the monolithic/hybrid on sapphire which is 34 times more expensive. Although the all monolithic design is not practical at the present time, the cost differential is pointed out to show the tremendous potential of monolithic microwave integrated antennas (MMIA's) in reducing production costs.

1.9 Recommendations

Based on the investigation summarized in the previous sections, the monolithic design offers potentially significant repeatability, reliability and cost advantages over the other candidate techniques. In terms of performance it is reasonable to assume that at worst the array efficiency will be comparable to the other design approaches, but with the added benefit of broad beamwidth and wide bandwidth element characteristics associated with high dielectric constant materials.

Although pursuit of this technology is consistent with our interpretation of the program objective, functional hardware cannot be implemented in this program in view of the extensive process development effort required. Therefore, we recommend

that monolithic microwave integrated antenna technology be developed on future programs both at 15 GHz and higher millimeter frequencies.

In order to fulfill the immediate requirements of this program, however, we have selected the monolithic/hybrid approach on a high dielectric constant material, specifically sapphire. This choice takes advantage of the simple fabrication and assembly procedures while maintaining the benefits of the microstrip radiator on a high K material. Such a design concept is also a logical precursor in the evolution of MMIA's since both silicon-on-sapphire and Gallium Arsenide-on-sapphire are established semiconductor technologies. Although the losses are higher with the selected design, we feel that this is only a temporary shortcoming. The ultimate successor to this design, MMIAs, will reduce losses by employing more efficient phase shifters with the added feature of including distributed amplifiers to compensate for losses or provide gain.

2.0 TEST RESULTS

As previously discussed, the investigation concerning antenna patches on various high permittivity materials lead to the conclusion that future experimental circuits should be fabricated on sapphire rather than on alumina because of sapphire's lower losses. A complication arises using monocrystalline sapphire substrates because the material is uniaxially anisotropic. However, using substrates cut in a particular orientation causes a material permittivity that is constant everywhere in the plane of the material. Microstrip theory can then be applied providing the relative permittivity is replaced with an isotropic-substrate relative permittivity which is a function of w/h of the microstrip lines. [7]

The general direction of the experimental work was to investigate various circuit configurations that would ultimately lead to a steerable, hybrid antenna array. Thus, the first step was to fabricate a 1x4 broadside array and to evaluate its performance. Subsequent steps involved optimizing the microstrip circuitry.

Besides the array fabrication, work was done to create a preliminary phase shift network. This involved the design of a 3-dB branch line coupler which would operate at the high design frequency. The coupler was chosen as a viable phase shift method because, as mentioned previously, less diodes were involved than in more conventional methods.

Circuit fabrication techniques paralleled those techniques used for digital I.C. fabrication except that only single layer designs instead of multi-layer designs were created. The desired microstrip circuit was designed to fit onto either a 1 square inch or 4 square inch substrate, then digitized into rectangular coordinates. A paper tape containing the informa-

tion was then punched and fed into a Gyrex pattern generator which created a photographic plate of the microstrip circuit. The precision glass plates were necessary to insure consistent widths in the high impedance lines and clean, clearly defined junctions and corners. With conventional film negatives, very thin feedlines tend to vary in width due to lower resolution, warpage and imperfect contact with the substrate. In addition, the film negative will only be as accurate as the camera that created it. However, the plates maintained the accuracy of the pattern generator which was approximately one-tenth of a mil. After etching, the completed substrate was soldered onto a copper block which acted as an extended ground plane for the circuit and end launch connectors were attached which served as the interface between the circuit and the test equipment.

2.1 The Antenna Array

2.1.1 First Iteration of the 4x4 Array

The first 4x4 array comprised a relatively straightforward layout design. Each antenna was placed such that its upper left corner was 0.48λ from the upper left corner of any of its immediate neighbors. The antenna patch itself was one previously designed. A computer plot and a photograph of this 4x4 array appear in Figures 23 and 24. Upon inspection of the plot, it can be seen that mitered corners were not employed for the design since the design was to act as a first approximation only.

After fabrication of the above design, the VSWR and the radiation patterns of the array were recorded. What was construed from the resulting VSWR was that element and transformer mismatches had occurred and had caused an unfavorable VSWR at the design frequency of 15 GHz. Mismatch and transmission line losses were also indicated by the radiation patterns taken.

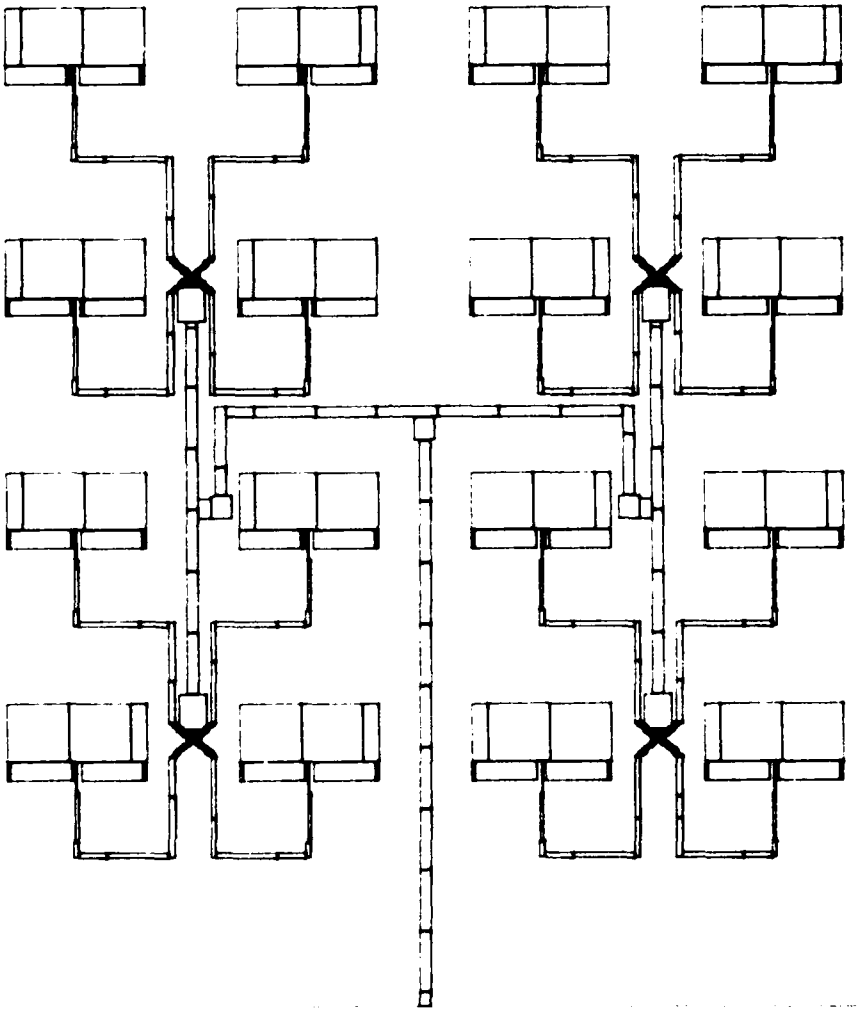


Figure 24. Computer Graphics Plot Of Original 4x4 Array

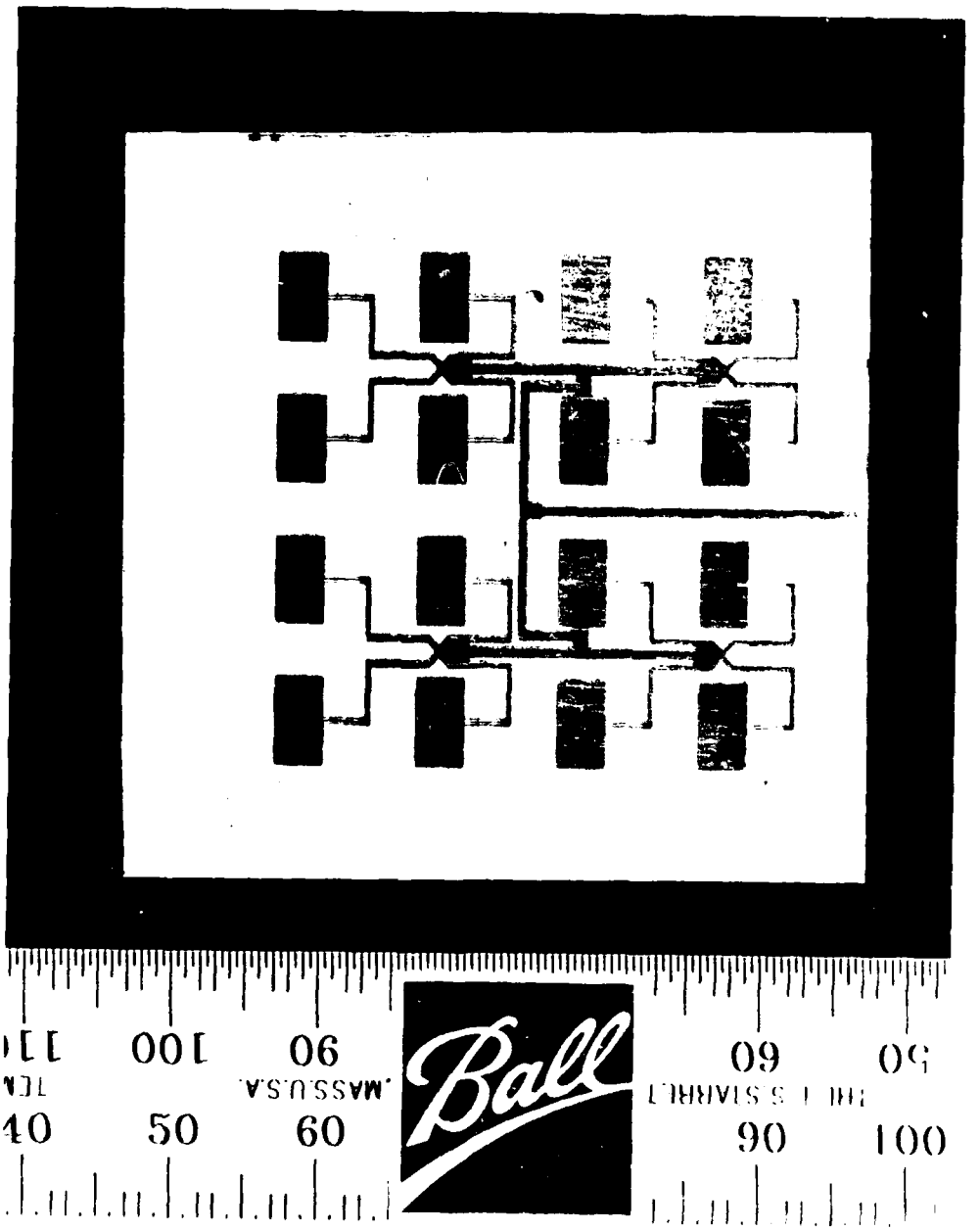


Figure 24. 15 GHz 4x4 Array

Although the patterns for the E and H-plane polarizations seemed to exhibit a good deal of directivity (approximate beamwidths of 35° and 50°, respectively, across the measured frequency range of 14.9 to 16.1 GHz), the gain was substantially lower than the anticipated 14.7 dB gain estimated for the array; this estimate was based on the beamwidth measurement. Samples of an E and H-plane radiation pattern for a frequency of 15.5 GHz are shown in Figures 25 and 26. These patterns are typical of the type taken across the measured frequency range. Because of the low gain, substantial losses were probably incurred through transmission line losses and antenna patch mismatches. Also, coupling between antennas 3-2 and 3-3 (matrix notation) and the quarter-wave transformers used to feed the 2x4 sections was believed to have taken place as evidenced by the lower than anticipated side lobe levels at some frequencies.

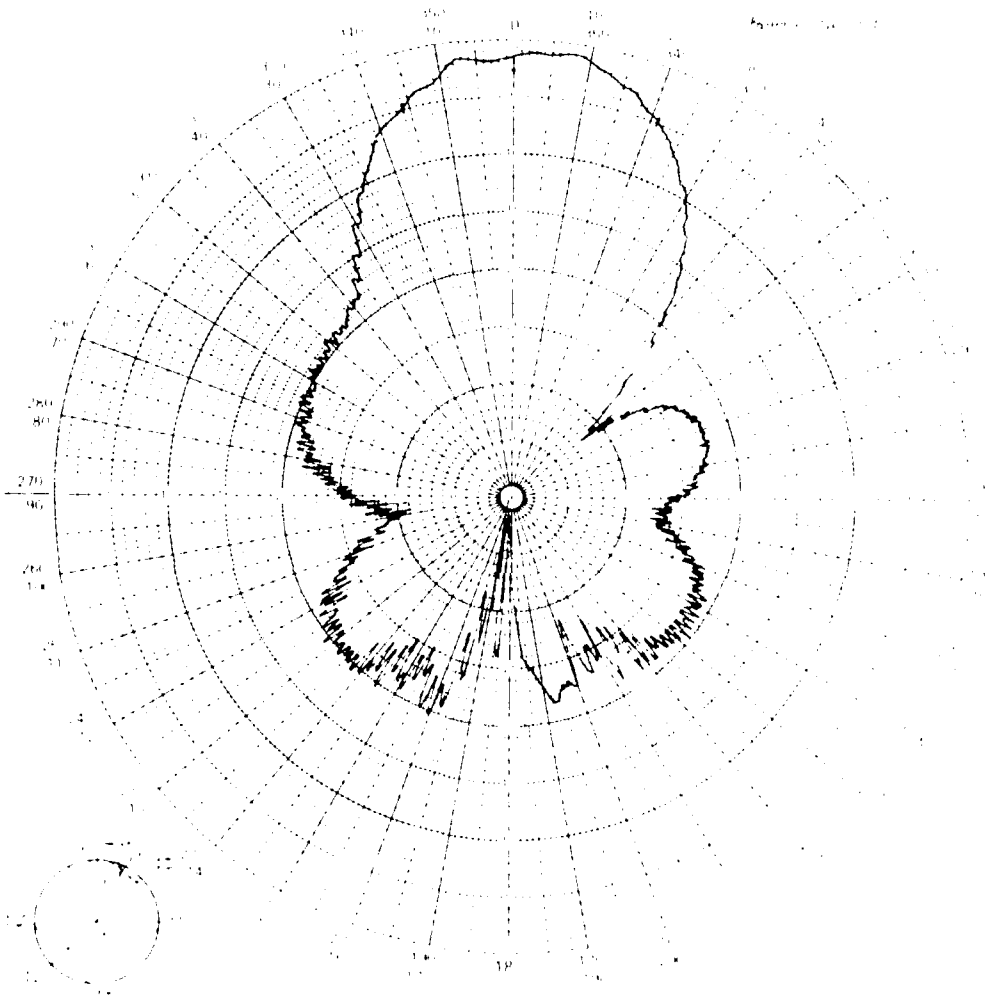
2.1.2 First Iteration of the 2x2 Array

In an effort to isolate loss contributions, the original 4x4 array was broken down into separate pieces: the main transformer network used to feed the two 2x4 arrays, the secondary transformer which fed each of the four 2x2 arrays and the 2x2 array.

The 2x2 array was tested for VSWR and for radiation patterns. The resulting VSWR showed the array to suffer from serious mismatch error throughout most of the measured frequency range. The radiation patterns showed less directivity than the 4x4 (E-plane polarization beamwidth was typically 65°). Thus, it was concluded that any favorable impedance matches of the 4x4 array were due mostly to combinations of errors.

ANTENNAS

PROJECT NO		PROGRAM			
PART NO	MODEL NO		SERIAL NO		
FREQUENCY		RANGE	[ ] LG	[ ] SM	[ ] OTHER
TEST TYPE:	[ ] DEVELOPMENT	[ ] PRE	[ ] FINAL		
PATTERN IN DB	DB (ON CHART) = 0 DBI		SHEET	OF	



ORIENTATION

REMARKS

POLARIZATION

OPER

WITNESSED

DATE

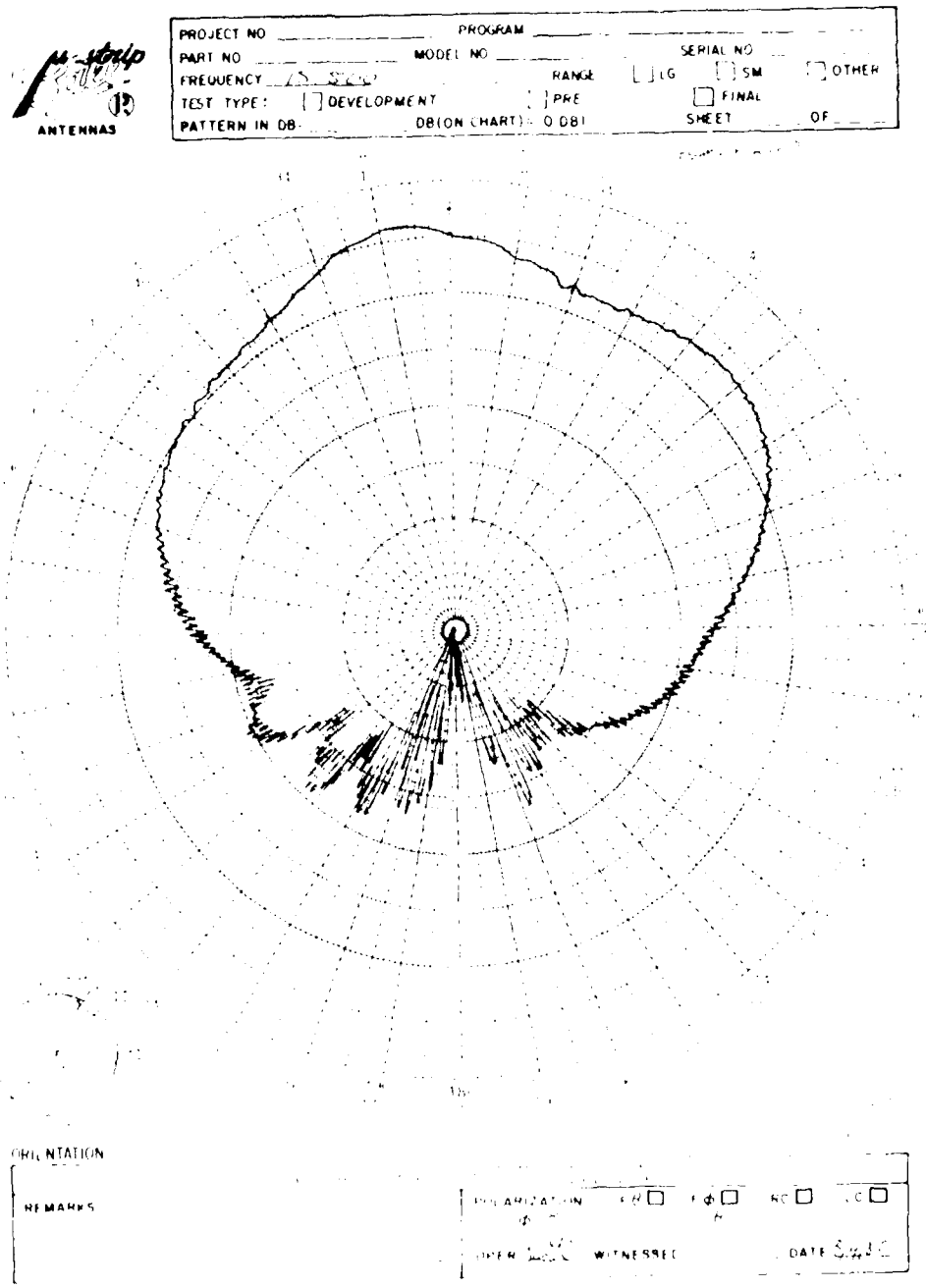


Figure [illegible] Radiation Pattern at [illegible] GHz

2.1.3 Second Iteration of the 2x2 Array

Using the results of the tests made on the original 2x2 array, several design changes were made and incorporated in the next generation 2x2 array.

The first change involved the redesign of the antenna patch. Because the antenna design chosen for the array had been designed for use on a slightly thinner substrate, the size of the patch was reduced by 6.0%, 6.5%, and 7.0% to provide three new antennas to be tested on the slightly thicker substrate. Subsequent VSWR measurements revealed the 6.5% smaller antenna to be the optimal design of the three; its measured VSWR was within 2:1 for frequencies ranging from 14.49 GHz to 15.24 GHz. The VSWR of this antenna patch is shown in Figure 27.

Another change involved the layout of the array. In order to avoid as much coupling as possible, the transformer used to feed the 2x2 sections was moved from its close proximity to the bottom two antennas of the section (see Figure 23) to a new location in the center of the 2x2 section. Feedline paths were then altered to preserve the equal phasing of antenna patches. This new layout of the 2x2 array is shown in Figure 28.

A third change to the original array was to use mitered, or angled, corners instead of the 90° corners first used. In order to accomplish this, these diagonal sections consisted of small rectangular boxes centered about the desired diagonal lines because the pattern generator used to create the masks of the designs could move only in x-direction or y-direction increments. Thus, direct diagonal lines were not possible. A section of the 2x2 array computer plot was magnified to show the details of the diagonal corners and is shown in Figure 29. This figure also shows the details of the 4:1 power divider used to feed the 2x2 array.

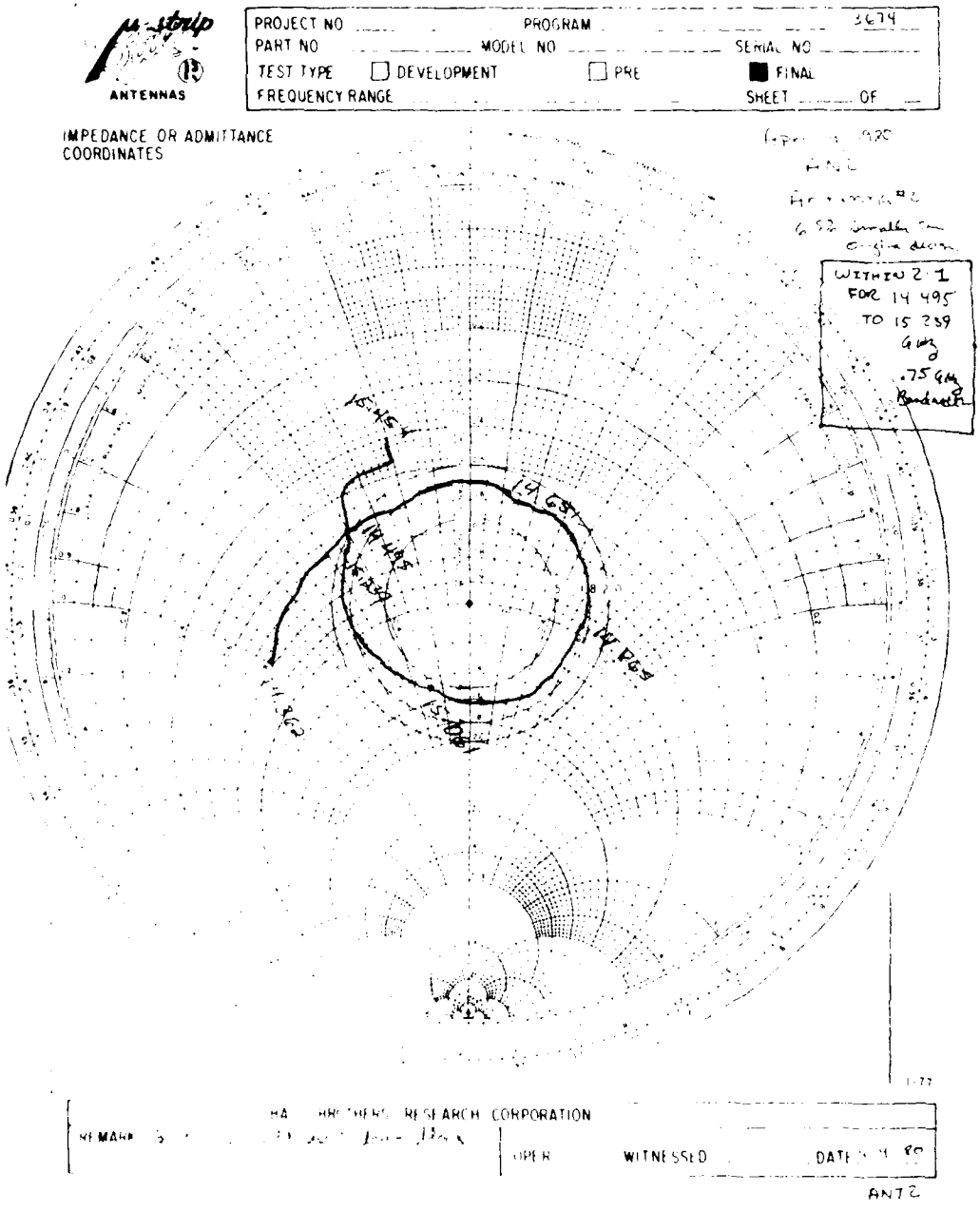


Figure [illegible] Antenna Patch Used In Subsequent Arrays

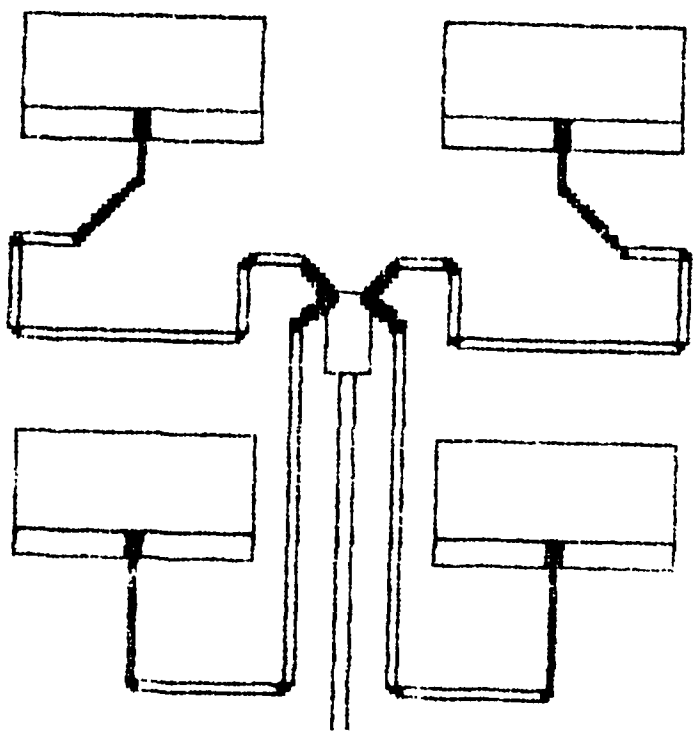


Figure 28. Computer Graphics Plot Of Second Iteration 2x2 Array

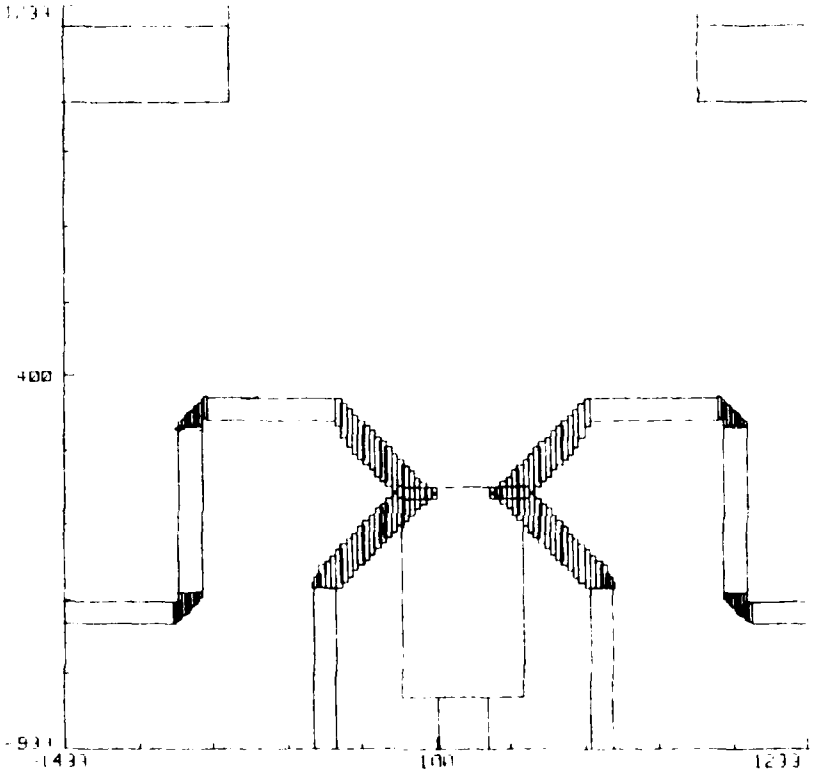


Figure 29. Computer Graphics Plot Of Corner Details

The 4:1 power divider was a redesign of the power divider originally used. The change involved cleaner intersections between the transformer and its four branches of transmission line.

The last design change was to increase the separation between the antenna patches from .48λ to .50λ. This increase of approximately 25 mils was done to provide more room between the transmission lines and the patches.

VSWR and radiation patterns were taken for the new array. The VSWR was measured for a frequency range of 14.0 to 16.0 GHz. The VSWR showed considerable improvement over the first array and is shown in Figure 30.

The radiation patterns had typical beamwidths of 50° in the H-plane and 40° in the E-plane. These beamwidths predict just under 10 dB of gain for the array; the measured gain was approximately 9 dB. With intrinsic conductor losses averaging .3 dB/-inch and approximate transmission line lengths totalling three inches, then nearly a dB can be attributed to line losses.

2.1.4 Second Iteration of the 4x4 Array

The design of a subsequent 4x4 array would have used the 2x2 array as a model for each of the quadrants. The top two quadrants would exactly be the 2x2 and the bottom two quadrants would be the 2x2 varied slightly to accommodate the positioning of the 4:1 power divider such that all feedline paths would be of equal length. It was felt that the modifications to standard fabrication techniques discussed above were the steps necessary to assure that the final 4x4 element array would perform as expected.

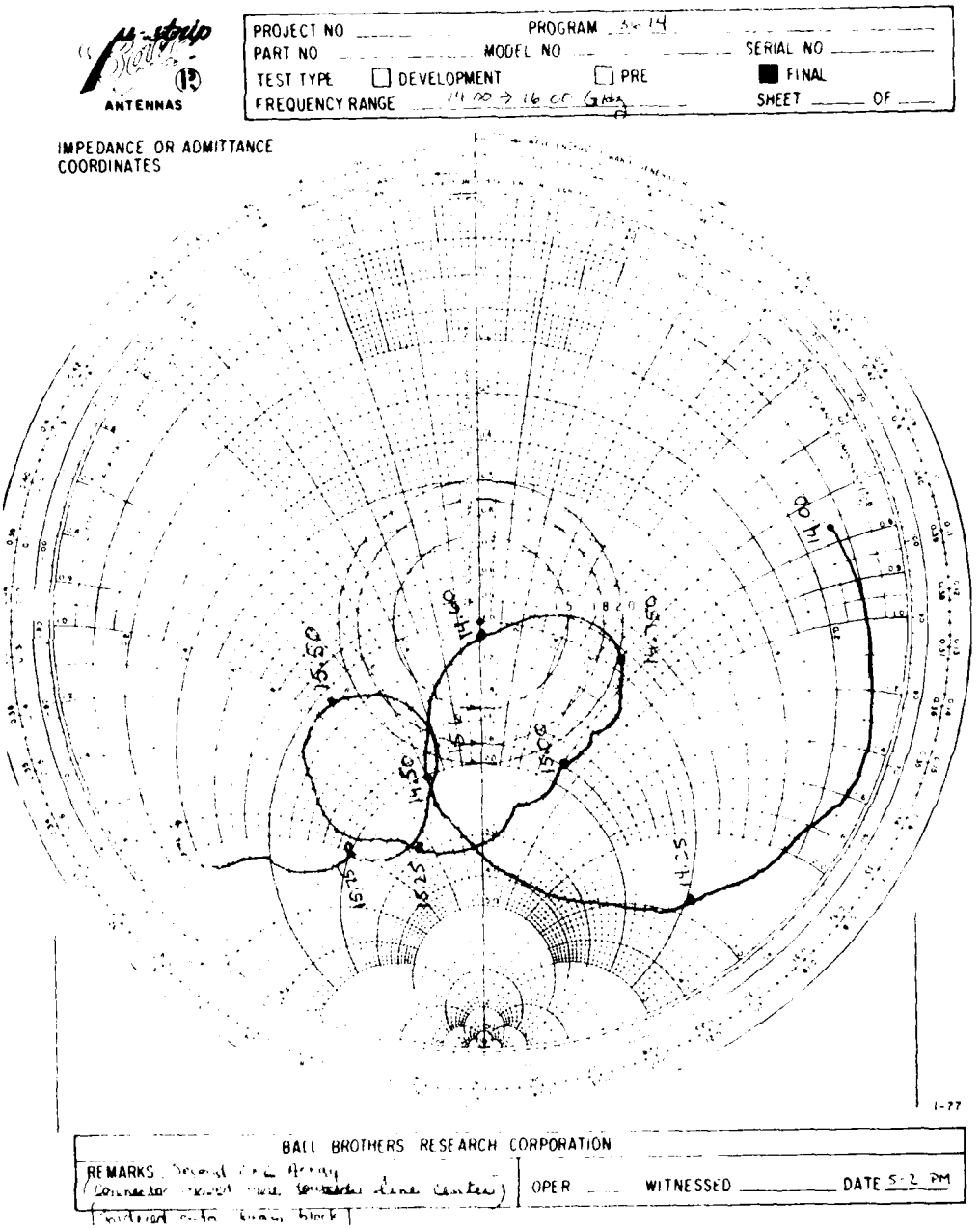


Figure 30. VSWR Of Second Iteration of 2x2 Array

2.2 The 3-dB Branch Line Coupler

The three decibel directional coupler was to be the basic building block for the 180° and 90° phase bits in the 3-bit phase shifter. Thus, the first step in creating a suitable switching network involved the development of an adequate 3-dB branch line coupler. An iterative process that allowed two slightly different coupler models to be fabricated on a single substrate was used in the coupler development.

2.2.1 First Iteration of the Coupler

A straightforward design approach was initially used. Shunt and series legs of the first model were designed to be a quarter wavelength in length as measured from the centers of each respective T-junction. A computer plot of the coupler is shown in Figure 31. The quarter wavelengths were determined specifically for the respective resistances of the shunt and series legs.

In the second model, the shunt legs were placed slightly further apart, resulting in an increase in the length of the series legs; all else remained unchanged. It was hoped changing only one variable would cause a resultant change in coupler performance that would give an insight as to what changes should be made for optimization.

Test results for the first iteration indicated that the two equal amplitude ports tracked each other better when the series legs were slightly longer; however, resultant signal levels were lower than anticipated. The VSWR indicated the high loss was due to impedance mismatch. Also, the measured phase between the two matched ports was greater than the desired 90° phase difference.

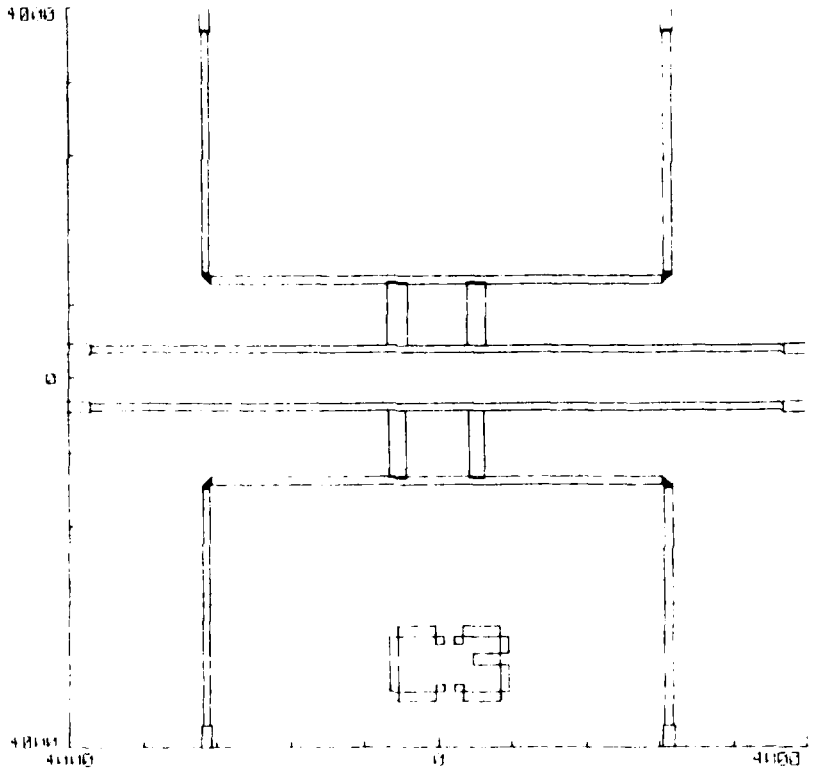


Figure 31. Computer Graphics Plot of 3-dB Coupler

2.2.2 Second Iteration of the Coupler

A new design based on the aforementioned results was utilized for the second iteration. Both the series legs and the shunt legs were shortened slightly.

The results from this design showed a marked improvement over the previous iteration. The two equal amplitude ports tracked within one decibel of each other for frequencies ranging from 14.50 GHz to 15.25 GHz; the isolated port signal was just under 20 dB down from the input signal. However, the phase between the two equal amplitude ports measured only 80°.

Phase measurements were, perhaps, the most sensitive measurement techniques since each mil of length corresponded to approximately one degree of phase change.

There are various methods to verify the validity of coupler measurements. One method for verifying the validity of the amplitude and VSWR measurements is to sum the output power of each port and to compare that number to the input power. A summation of the output powers plus the approximate line losses for the second iteration are shown in Table 5. Because this tabulation accounts for 95% of the input power, it can be assumed the measurements made were valid. To check the validity of the phase measurements, one can measure the insertion loss between the input and isolated ports with the two equal amplitude ports first short circuited then open circuited. If the approximately correct phase relationship exists in the coupler square, then the results of these two measurements should be nearly equal.

A test of this nature was performed on the coupler. The test results showed that although the data from a shorted and open circuit tracked each other, the amplitudes, on the average,

were approximately 2.5 dB apart. However, other test data showed that the amplitudes differed by only 1 dB at a frequency somewhat higher than the design frequency. These results indicated the two ports were under 90^{0} apart; this coincided with data gathered from the phase measurements.

TABLE 5

Total Power As Measured On Second Iteration

Coupler At Design Frequency

Power As Measured AT	Measured Power (dB)	Percentage of Total Power
Input Port (Reflected Pwr)	-17.8 dB	2
Isolated Port	-18.0 dB	2
3 dB Port A	-3.8 dB	42
3 dB Port B	-5.0 dB	32
Total Power Measured		78
Estimated Losses	0.8 dB	17
Total Power Accounted For		95

2.2.3 Third Iteration of the Coupler

For the third iteration, one of the models was designed using a set of equations which took T-junction effects into account. [8] T-junction discontinuities, which can usually be ignored at lower frequencies, become more prominent at higher frequencies because their size is no longer negligible as compared to wavelength.

A summary of the results of the equations is as follows: at high frequencies the parasitic capacitances caused by the T-junction formed between a high impedance line and a lower impedance line causes the high impedance line to appear shorter in length and the lower impedance line to appear equally longer in length. Also, the effective impedances of series and shunt legs are affected by the discontinuities. The shunt leg impedance appears slighly higher while the series leg impedance appears just barely lower than the original value.

Thus, in this iteration model, the shunt legs were decreased in length by five degrees and the series legs were equally increased. Also, the shunt impedance was lowered to forty-five ohms, while the series leg impedance was not altered.

Test results were encouraging. They showed however, that the coupler was fairly well matched at a higher than design frequency. Thus, the next iteration (had time allowed) would have had changes that were half the line length changes made from the second to third iteration.

2.3 Recommendations for Further Studies

An important area that warrants closer study concerns the developement of optimal guidelines for designing T-junctions, corners, transformers, line connections and other such similar

items. Standard layouts were used in this project, and it would be interesting to isolate each of the aforementioned, test its VSWR and modify the design until the best matched condition occurs.

New testing techniques that would allow for more accurate and repeatable test data would also be a desirable path of study. The testing technique would have to accomplish the following:

1. There must be adequate contact between the ground plane of the substrate and an extended ground plane in the form of a copper block.

2. Connectors leading to test equipment must be firmly attached to the input/output feedlines of the circuit to prevent impedance mismatches.

3. The top of the substrate must interface directly with air.

4. All connections must be consistently made.

Although the testing technique used accomplished the first three requirements adequately, improvement can be made in the area of consistency of contact between circuit ports and test equipment.

A third area that should be under consideration would involve an investigation of techniques other than the 3 dB coupler to accomplish the phase shift capabilities of the array. One method might be the use of backward wave couplers. The use of this type of coupler would avoid some of the problems connected with termination compensation, or meander-folded couplers could be investigated as they could represent a significant space saving device.

REFERENCES

[1] R. E. Munson, et al, "Microstrip Communications Antenna", Final Report RADC Contract F 30602-74-C 0298, pp. 2-22a, January 1976.

[2] G. G. Sanford, L. Klein, "Increasing the Beamwidth of A Microstrip Radiating Element", IEEE Antennas and Propagation International Symposium Digest, pp. 126-129, June 1979.

[3] "SHF SATCOM Microstrip Phased Array", Interim Technical Report RADC Contract F 30602-79-C-0241, Appendix A, May 1980.

[4] A. G. Derneryd, A. G. Lind, "Extended Analysis of Rectangular Microstrip Resonator Antennas", IEEE Trans. Antennas Propagation, Vol. AP-27, No. 6, pp. 846-849, November 1979.

[5] F. W. Cipolla, et al, "Microstrip Phased Array Antennas", Final Report RADC Contract F 30602-79-C-0137, pp. 103-110, May 1977.

[6] R. V. Garver, "Broadband Diode Phase Shifters", Harry Diamond Laboratory Technical Report HDL-TR-1562, August 1971.

[7] E. C. Edwards, R. P. Owens, "2-18 GHz Dispersion Measurements On 10-100 Ohm Microstrip Lines On Sapphire," IEEE Trans. Microwave Theory and Techniques, Vol. MTT-24, No. 8, pp. 506-513, August 1976.

[8] M. Dydyk, "Master the T-Junction And Sharpen Your MIC Designs", Microwaves, pp. 134-136, May 1977.

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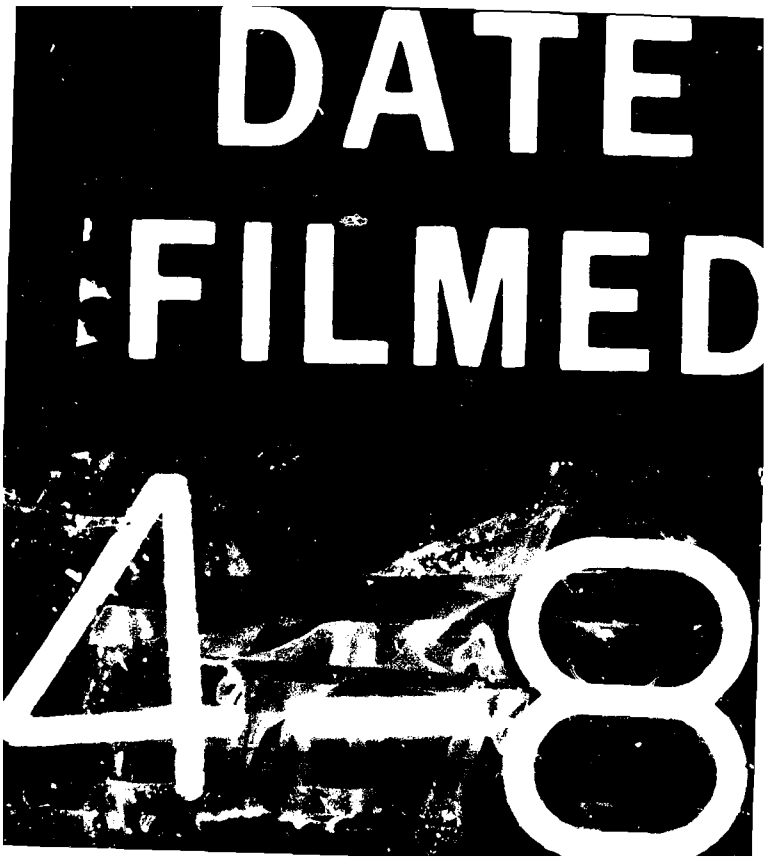
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